1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM,X646,MLB

X646 MLB

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2016-10-06

LAST_MODIFICATION=Thu Oct 6 17:00:29 2016

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36	39	ETHERNET: PHY (CAESAR IV)	FIYIN	01/19/2016
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38	41	SD CARD: Connector	FIYIN	01/19/2016
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80	92	GFX: GDDR5 FRAME BUFFER A	PETE	08/30/2016
81	93	GFX: GDDR5 FRAME BUFFER B	PETE	08/30/2016
82	94	GFX: GDDR5 FRAME BUFFER C	PETE	08/30/2016
83	95	GFX: GDDR5 FRAME BUFFER D	PETE	08/30/2016
84	96	GFX: DisplayPort INTF	PETE	07/17/2016
85	97	GFX: GPU GPIOS/PLLS/VBIOS ROM	PETE	07/17/2016
86	98	GFX: GPU STRAPS/TEMP SENSORS	PETE	02/19/2016
87	99	GFX: GPU GNDS	PETE	02/16/2016
88	101	GRAPHICS: GPU CORE VR	SUNIL	10/06/2016
89	102	GRAPHICS: GPU CORE VR (PHASES 1-3)	sunil	07/11/2016
90	103	GRAPHICS: GPU CORE VR (PHASES 4-6)	SUNIL	07/15/2016
91	104	GRAPHICS: GPU VDDQ VR	SUNIL	07/18/2016
92	105	GRAPHICS: GPU VDDCI VR	SUNIL	05/31/2016
93	106	GRAPHICS: GPU 0V8 VR	SUNIL	06/06/2016
94	107	GRAPHICS: GPU 1V8 VR	SUNIL	07/14/2016
95	108	GRAPHICS: GPU CORE PCC	SUNIL	08/23/2016
96	109	GRAPHICS: GPU VR MISC	sunil	01/13/2016
97	110	Power Connectors/Aliases	sunil	11/06/2015
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DRAWING

TITLE=X646_MLB
ABBREV=DRAWING
LAST_MODIFIED=Thu Oct 6 17:00:29 2016

SCHEM,X646,MLB

DRAWING TITLE: SCHEM, MLB, X646

Apple Inc.

DRAWING NUMBER: 051-01506 | SIZE: D

REVISION: 5.19.0

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DRAWING

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
985-00160	PCBA,DEV,MLB,X646	DEVELOPMENT,X646_DEVEL
685-00106	PCBA,MLB,COMMON PARTS,X646	X646_COMMON
639-03362	PCBA,MLB,CTO,EL XTA,VRAM_SAMSUNG,8GB,X646	X646,MLB_CMNPTS,CPU:CTO,GPU_SKU:EL_XTA,GPU:EL,FB_8G_SAM_EL,EEEE:HNL6,TRANS:DLT,ENET:TRANS
639-03363	PCBA,MLB,CTO,EL XTA,VRAM_HYNIX,8GB,X646	X646,MLB_CMNPTS,CPU:CTO,GPU_SKU:EL_XTA,GPU:EL,FB_8G_HYN_EL,EEEE:HNL7,TRANS:DLT,ENET:TRANS
639-03364	PCBA,MLB,CTO,EL XTA,VRAM_MICRON,8GB,X646	X646,MLB_CMNPTS,CPU:CTO,GPU_SKU:EL_XTA,GPU:EL,FB_8G_ELP_EL,EEEE:HNL8,TRANS:DLT,ENET:TRANS
639-03365	PCBA,MLB,ULT,EL PROA,VRAM_SAMSUNG,4GB,X646	X646,MLB_CMNPTS,CPU:ULT,GPU_SKU:EL_PROA,GPU:EL,FB_4G7_SAM_EL,EEEE:HNL9,TRANS:DLT,ENET:TRANS
639-03366	PCBA,MLB,ULT,EL PROA,VRAM_HYNIX,4GB,X646	X646,MLB_CMNPTS,CPU:ULT,GPU_SKU:EL_PROA,GPU:EL,FB_4G7_HYN_EL,EEEE:HNLC,TRANS:DLT,ENET:TRANS
639-03367	PCBA,MLB,ULT,EL PROA,VRAM_MICRON,4GB,X646	X646,MLB_CMNPTS,CPU:ULT,GPU_SKU:EL_PROA,GPU:EL,FB_4G7_ELP_EL,EEEE:HNLD,TRANS:DLT,ENET:TRANS
639-03368	PCBA,MLB,BEST,EL LEA,VRAM_SAMSUNG,4GB,X646	X646,MLB_CMNPTS,CPU:BEST,GPU_SKU:EL_LEA,GPU:EL,FB_4G7_SAM_EL,EEEE:HNLF,TRANS:TDK,ENET:TRANS
639-03369	PCBA,MLB,BEST,EL LEA,VRAM_HYNIX,4GB,X646	X646,MLB_CMNPTS,CPU:BEST,GPU_SKU:EL_LEA,GPU:EL,FB_4G7_HYN_EL,EEEE:HNLG,TRANS:TDK,ENET:TRANS
639-03370	PCBA,MLB,BEST,EL LEA,VRAM_MICRON,4GB,X646	X646,MLB_CMNPTS,CPU:BEST,GPU_SKU:EL_LEA,GPU:EL,FB_4G7_ELP_EL,EEEE:HNLH,TRANS:TDK,ENET:TRANS
639-03371	PCBA,MLB,BETTER,BF XPA,VRAM_SAMSUNG,2GB,X646	X646,MLB_CMNPTS,CPU:BTR,GPU_SKU:BF_XPA,GPU:BF,FB_4G7_SAM_BF,EEEE:HNLJ,TRANS:TDK,ENET:TRANS
639-03372	PCBA,MLB,BETTER,BF XPA,VRAM_HYNIX,2GB,X646	X646,MLB_CMNPTS,CPU:BTR,GPU_SKU:BF_XPA,GPU:BF,FB_4G7_HYN_BF,EEEE:HNLK,TRANS:TDK,ENET:TRANS
639-03373	PCBA,MLB,BETTER,BF XPA,VRAM_MICRON,2GB,X646	X646,MLB_CMNPTS,CPU:BTR,GPU_SKU:BF_XPA,GPU:BF,FB_4G7_ELP_BF,EEEE:HNLL,TRANS:TDK,ENET:TRANS
639-02813	PCBA,MLB EL,TEST BOARD,X646	X646,MLB_CMNPTS,GPU:EL,EEEE:HD97,TRANS:DLT,ENET:TRANS
639-02970	PCBA,MLB BF,TEST BOARD,X646	X646,MLB_CMNPTS,GPU:BF,EEEE:HHCG,TRANS:TDK

BOM Groups

BOM GROUP	BOM OPTIONS
X646_COMMON	COMMON,ALTERNATE,X646_PROGPARTS,XDP,CPU_DRMOS:CURRENT,GPUCLK:OSC,SSD:Y,VR_BULKCAP:CURRENT,1V8_AUDIO_DLY:N
X646_PROGPARTS	SMC:PROG,BOOTROM:PROG,TBTROM:PROG,CIVROM:PROG,CAMROM:PROG
X646_DEVEL	XDP_CONN,T112
FB_8G_SAM_EL	FB_BD_8G:SAM,FB_AC_8G:SAM,VR_VRAM_SAM_1V55
FB_8G_ELP_EL	FB_BD_8G:ELP,FB_AC_8G:ELP,VR_VRAM_ELP_1V50
FB_8G_HYN_EL	FB_BD_8G:HYN,FB_AC_8G:HYN,VR_VRAM_HYN_1V50
FB_4G7_SAM_EL	FB_BD_4G7:SAM,FB_AC_4G7:SAM,VR_VRAM_SAM_1V50
FB_4G7_ELP_EL	FB_BD_4G7:ELP,FB_AC_4G7:ELP,VR_VRAM_ELP_1V55
FB_4G7_HYN_EL	FB_BD_4G7:HYN,FB_AC_4G7:HYN,VR_VRAM_HYN_1V50
FB_4G7_SAM_BF	FB_BD_4G7:SAM,VR_VRAM_SAM_1V50
FB_4G7_ELP_BF	FB_BD_4G7:ELP,VR_VRAM_ELP_1V55
FB_4G7_HYN_BF	FB_BD_4G7:HYN,VR_VRAM_HYN_1V50

CPUs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S00344	1	CPU,KBL,QKHB,B0,QS,4.2,91W,1.15,L1151	CPU	CRITICAL	CPU:CTO
337S00345	1	CPU,KBL,QKHB,B0,QS,3.8,91W,1.15,L1151	CPU	CRITICAL	CPU:ULT
337S00343	1	CPU,KBL,QKHB,B0,QS,3.5,65W,1.15,L1151	CPU	CRITICAL	CPU:BEST
337S00340	1	CPU,KBL,QKHC,B0,QS,3.4,65W,1.1,L1151	CPU	CRITICAL	CPU:BTR

SOCKET& CONNECTOR

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S00002	1	CONN,CPU,SOCKET,LGA1151,SKYLAKE,HF	U0500	CRITICAL	
806-07339	1	COVER,SHIELD,USB-C,X635	EMI_SHIELD	CRITICAL	

ASICs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S00187	1	IC,PCH-H,SKL,SSKGU2170,SR2C9,D1,PRQ,BGB37	U1100	CRITICAL	
338S00254	1	IC,TBT,ALPINE RIDGE,SLL5M,PRQ,C1,CSP337	U2800	CRITICAL	
343S0616	1	IC,BCM57766A1,ENETGIGD,8X8	U3900	CRITICAL	
353S00961	2	IC,CD3215,ACE,C00,USB PWR SW,BLNK,BGA96	U3100,U3200	CRITICAL	

Programmable Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S00734	1	IC,EFI ROM,VTBD,EVT,X646	U5210	CRITICAL	BOOTROM:PROG
335S00006	1	IC,64 MBIT SPI SERIAL FLASH	U5210	CRITICAL	BOOTROM:BLANK
341S00568	1	IC,SMC-B1,EXTERNAL,VTBD,X646	U5000	CRITICAL	SMC:PROG
338S1214	1	IC,SMC12-B1,40MHZ/500MIPS,MCU,157BGA	U5000	CRITICAL	SMC:BLANK
341S00740	1	IC,AR,V9.3,EVT,X646	U2890	CRITICAL	TBTROM:PROG
335S00133	1	IC,SPI FLASH ROM,8MBIT,50MHZ,USON8	U2890	CRITICAL	TBTROM:BLANK
341S3912	1	IC,ENET ROM,NUMONYX,V1.15,J16/J16G/J17	U3990	CRITICAL	CIVROM:PROG
335S0854	1	1-MBIT,SPI FLASH ROM SOIC, HF	U3990	CRITICAL	CIVROM:BLANK
341S00667	1	IC,CAMERA,FLASH,V72.52,X646	U4202	CRITICAL	CAMROM:PROG
335S0852	1	IC,FLASH,SPI,1MBIT,3V3	U4202	CRITICAL	CAMROM:BLANK
341S00555	1	IC,GPU ROM,ELM,VTBD,X646	U9700	CRITICAL	GPUROM:PROG
335S0724	1	1MBIT SERIAL FLASH 2X3X0.6MM	U9700	CRITICAL	GPUROM:BLANK

Bar Code Labels / EEEE #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7896	1	LABEL,MLB,2D	EEEE_HNL6	CRITICAL	EEEE:HNL6
825-7896	1	LABEL,MLB,2D	EEEE_HNL7	CRITICAL	EEEE:HNL7
825-7896	1	LABEL,MLB,2D	EEEE_HNL8	CRITICAL	EEEE:HNL8
825-7896	1	LABEL,MLB,2D	EEEE_HNL9	CRITICAL	EEEE:HNL9
825-7896	1	LABEL,MLB,2D	EEEE_HNLC	CRITICAL	EEEE:HNLC
825-7896	1	LABEL,MLB,2D	EEEE_HNLD	CRITICAL	EEEE:HNLD
825-7896	1	LABEL,MLB,2D	EEEE_HNLF	CRITICAL	EEEE:HNLF
825-7896	1	LABEL,MLB,2D	EEEE_HNLG	CRITICAL	EEEE:HNLG
825-7896	1	LABEL,MLB,2D	EEEE_HNLH	CRITICAL	EEEE:HNLH
825-7896	1	LABEL,MLB,2D	EEEE_HNLJ	CRITICAL	EEEE:HNLJ
825-7896	1	LABEL,MLB,2D	EEEE_HNLK	CRITICAL	EEEE:HNLK
825-7896	1	LABEL,MLB,2D	EEEE_HNLL	CRITICAL	EEEE:HNLL
825-7896	1	LABEL,MLB,2D	EEEE_HD97	CRITICAL	EEEE:HD97
825-7896	1	LABEL,MLB,2D	EEEE_HHCG	CRITICAL	EEEE:HHCG

ALTERNATE PARTS TABLE LOCATED ON CSA 115

J135 SCHEMATIC / PCB #'S

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-01506	1	SCH,MLB,X646	SCH1	CRITICAL	X646
820-00609	1	PCBF,MLB,X646	PCB1	CRITICAL	X646
685-00106	1	PCBA,MLB COMMON PARTS,X646	CMNPTS	CRITICAL	MLB_CMNPTS

GPU and VRAM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S00277	1	IC,GPU,AMD,ELLESMERE,XTA,Q5,A1,LF,BGA1401	U8700	CRITICAL	GPU_SKU:EL_XTA
337S00279	1	IC,GPU,AMD,ELLESMERE,PROA,Q5,A1,LF,BGA1401	U8700	CRITICAL	GPU_SKU:EL_PROA
337S00347	1	IC,GPU,AMD,ELLESMERE,LEA,Q5,A1,LF,BGA1401	U8700	CRITICAL	GPU_SKU:EL_LEA
337S00346	1	IC,GPU,AMD,BAFFIN,XPA,A1,LF,Q5,BGA1401	U8700	CRITICAL	GPU_SKU:BF_XPA
333S00100	4	IC,GDDR5,8GBIT,7GBPS,20NM,BGA170	U9300,U9350,U9500,U9550	CRITICAL	FB_BD_8G:HYN
333S00100	4	IC,GDDR5,8GBIT,7GBPS,20NM,BGA170	U9200,U9250,U9400,U9450	CRITICAL	FB_AC_8G:HYN
333S00075	4	IC,GDDR5,8GBIT,7GBPS,20NM,BGA170	U9300,U9350,U9500,U9550	CRITICAL	FB_BD_8G:ELP
333S00075	4	IC,GDDR5,8GBIT,7GBPS,20NM,BGA170	U9200,U9250,U9400,U9450	CRITICAL	FB_AC_8G:ELP
333S00074	4	IC,GDDR5,8GBIT,7GBPS,20NM,BGA170	U9300,U9350,U9500,U9550	CRITICAL	FB_BD_8G:SAM
333S00074	4	IC,GDDR5,8GBIT,7GBPS,20NM,BGA170	U9200,U9250,U9400,U9450	CRITICAL	FB_AC_8G:SAM
333S00043	4	IC,GDDR5,4GBIT,7GBPS,25NM,BGA170	U9300,U9350,U9500,U9550	CRITICAL	FB_BD_4G7:HYN
333S00043	4	IC,GDDR5,4GBIT,7GBPS,25NM,BGA170	U9200,U9250,U9400,U9450	CRITICAL	FB_AC_4G7:HYN
333S00044	4	IC,GDDR5,4GBIT,7GBPS,25NM,BGA170	U9300,U9350,U9500,U9550	CRITICAL	FB_BD_4G7:ELP
333S00044	4	IC,GDDR5,4GBIT,7GBPS,25NM,BGA170	U9200,U9250,U9400,U9450	CRITICAL	FB_AC_4G7:ELP
333S00078	4	IC,GDDR5,4GBIT,7GBPS,20NM,BGA170	U9300,U9350,U9500,U9550	CRITICAL	FB_BD_4G7:SAM
333S00078	4	IC,GDDR5,4GBIT,7GBPS,20NM,BGA170	U9200,U9250,U9400,U9450	CRITICAL	FB_AC_4G7:SAM

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SYNC_MASTER=j135_mlb SYNC_DATE=06/28/2016

PAGE TITLE

BOM Configuration

Apple Inc.

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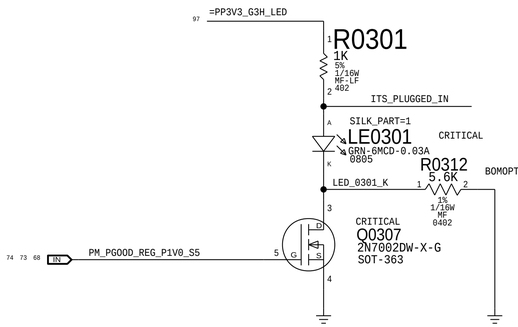
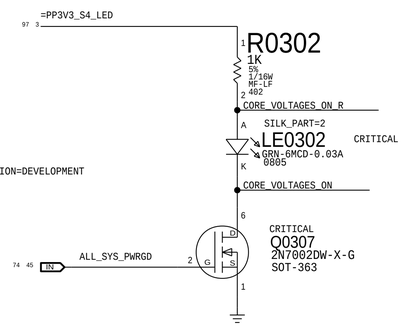
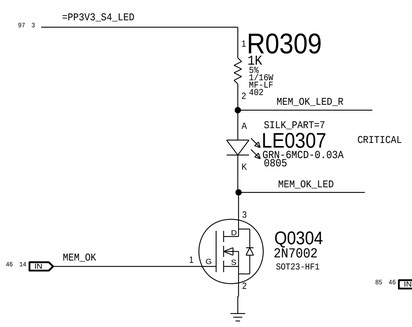
S5 Pwr LED



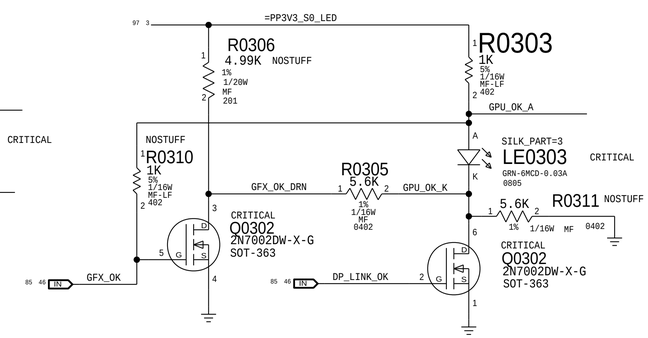
ALL_SYS_PWRGD LED



MEM_OK LED

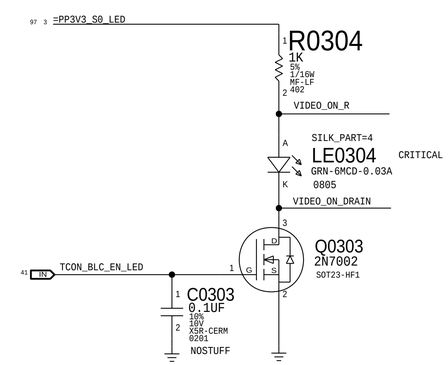


GPU OK LED

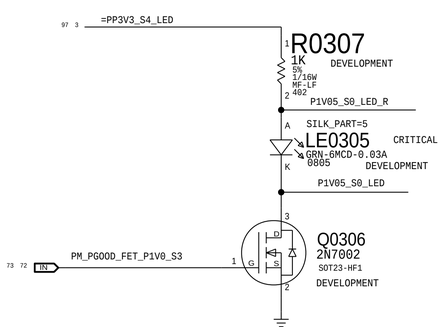


THIS LED IS DRIVEN BY GPU:
GFX_OK HIGH LIGHTS THE LED DIMLY
DP_LINK_OK HIGH LIGHTS THE LED FULLY

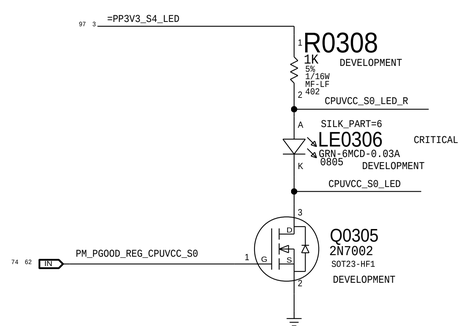
TCON OK LED



P1V0_S3_PWRGD LED



CPUVCC_S0_PWRGD LED



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SYNC_MASTER=ANDREW SYNC_DATE=02/18/2016

PAGE TITLE
DEBUG: LEDs

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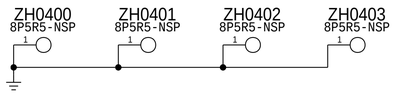
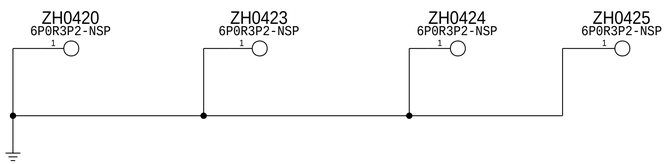
CPU Heatsink

4MM PLATED HOLES (998-4158)



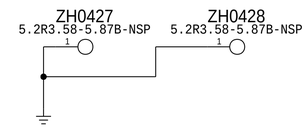
GPU HEATSINK MOUNTING FEATURES

(998-5013. PLATED HOLE, 3.2MM DIA, 6MM PAD TOP/BOT)



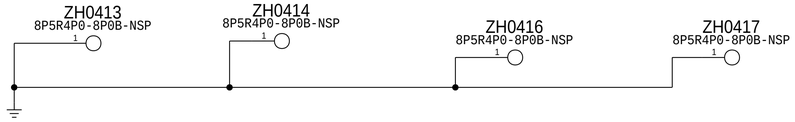
GPU HEATPIPE MOUNTING FEATURES

998-06191 (PLATED HOLES, 3.58MM INNER DIAMETER)



Rear Cover

998-5014 (PLATED HOLES, 4MM DRILL, 8.5MM TOP, 8MM BOT)



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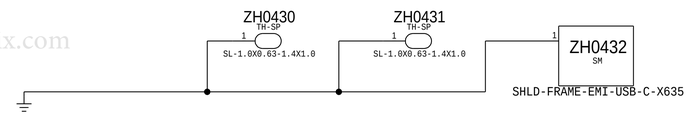
USB-C Alignment Holes and EMI Can

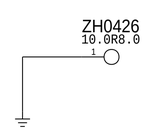


Rear Cover

860-5674 (PCB STANDOFF)

HEATPIPE MTG HOLES

998-5527 (PLATED HOLES, 8MM DIA, 10MM PAD)



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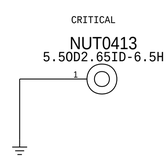
WIRELESS CARD MTG HOLES

998-06186 (PLATED HOLES, 3.3mm INNER DIAMETER, 5mm Top pad)

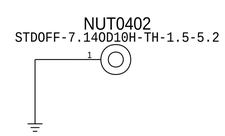
SSD STANDOFF

APN: 860-00314



LOL Boss

860-5675 (PLATED HOLE, 8.41mm pad Top, 8mm pad Bot)



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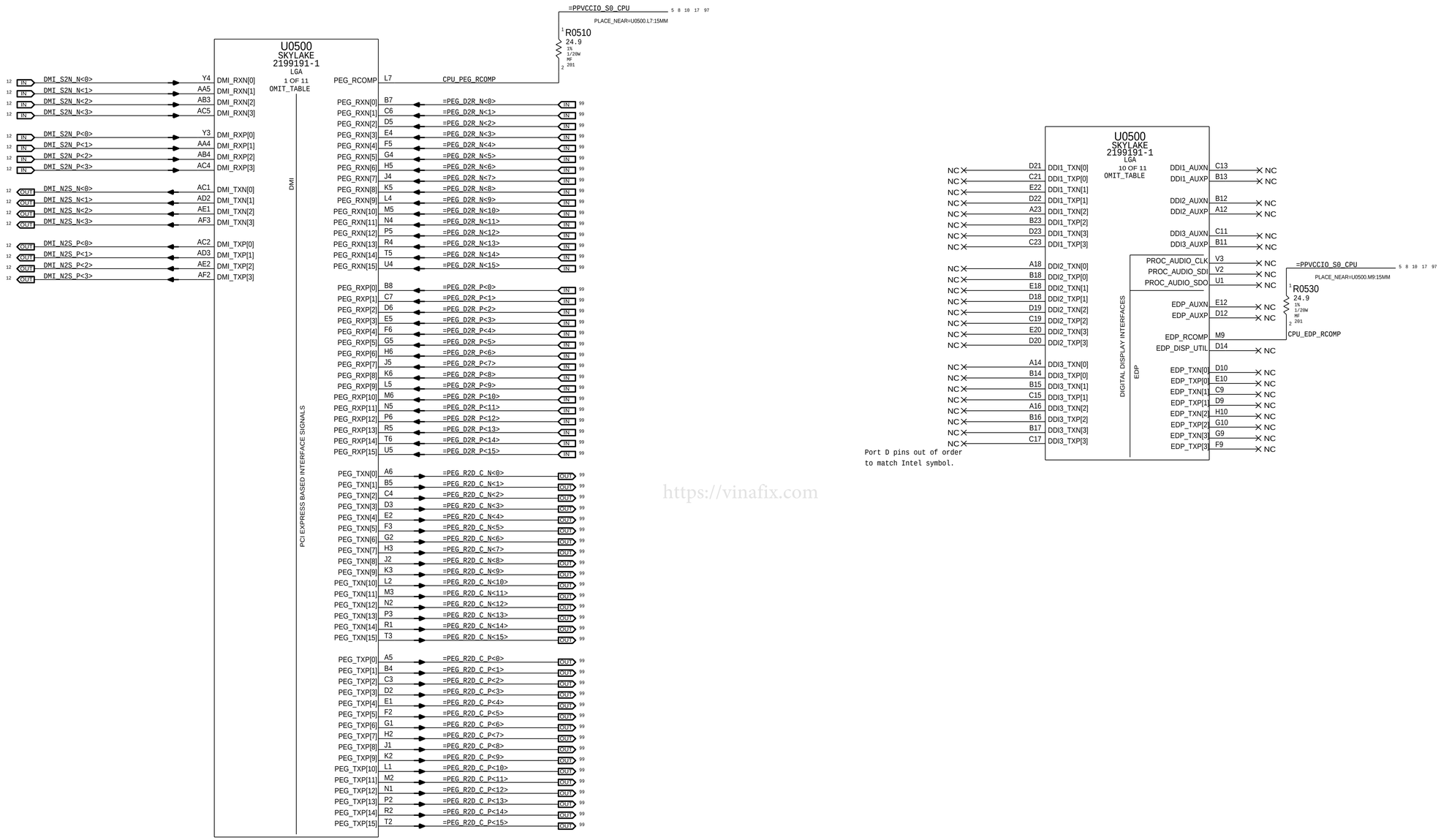

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SYNC_MASTER=D0RESSLER SYNC_DATE=02/03/2016

PAGE TITLE
CPU & CHIPSET: CPU DMI/PEG/FDI/RSVD

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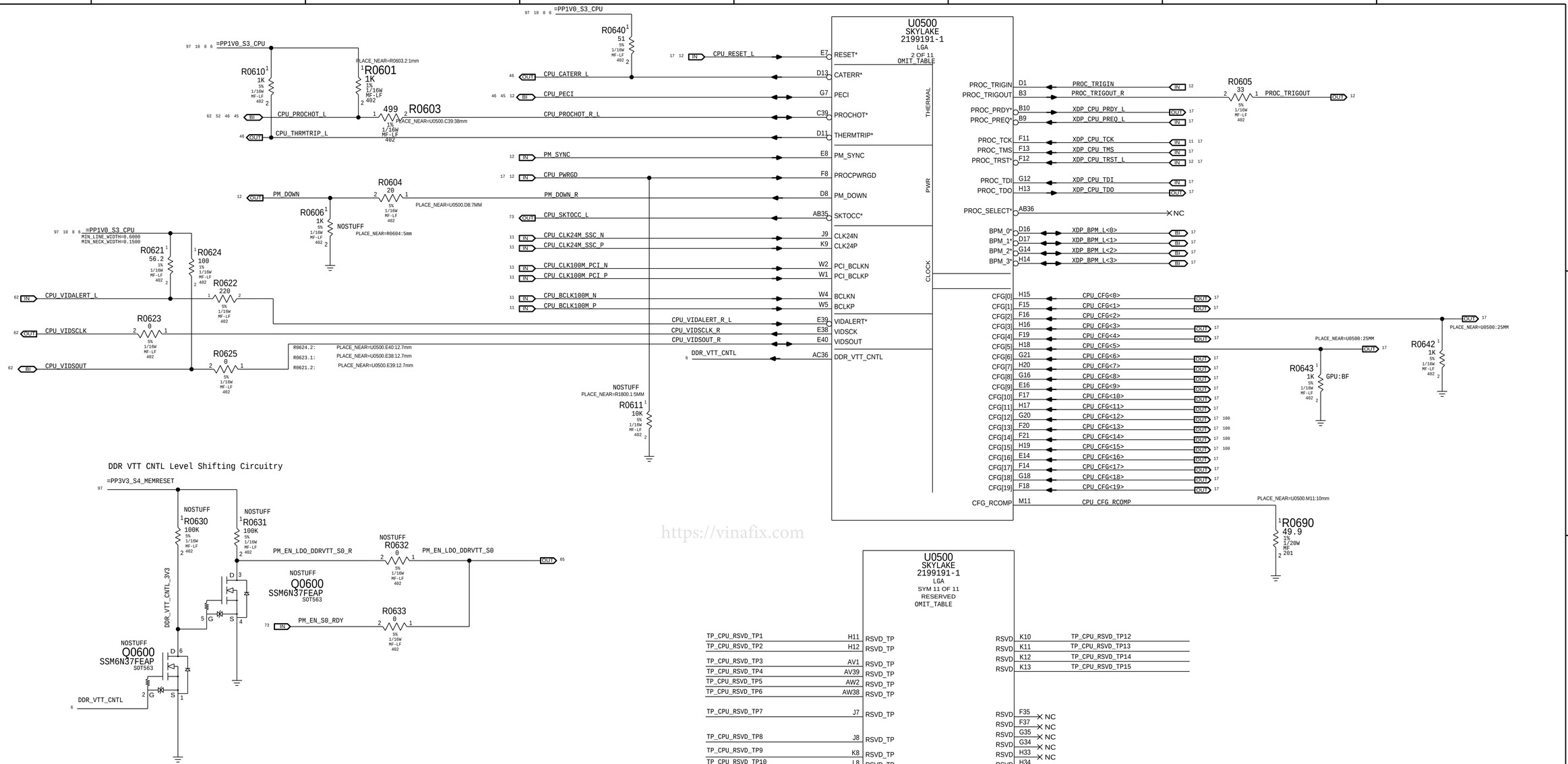

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Table 2-17. PCI Express* Bifurcation and Lane Reversal Mapping

Bifurcation	Link Width			Config. Signals			Lanes															
	0:1:0	0:1:1	0:1:2	CFG [6]	CFG [5]	CFG [2]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16	x16	N/A	N/A	1	1	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16 **Reversed**	x16	N/A	N/A	1	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2x8	x8	x8	N/A	1	0	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
2x8 **Reversed**	x8	x8	N/A	1	0	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1x8+2x4	x8	x4	x4	0	0	1	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
1x8+2x4 **Reversed**	x8	x4	x4	0	0	0	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

Notes:
1. For CFG bus further details, refer to Section 6.4.
2. Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
3. In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
   — Connect lane 0 of 1st device to lane 0.
   — Connect lane 0 of 2nd device to lane 8.
   — Connect lane 0 of 3rd device to lane 12.

   For example:
   a. When using 1x8 + 2x4, the 8 lane device must use lanes 0:7.
   b. When using 1x4 + 1x2, the 4 lane device must use lanes 0:3, and other 2 lanes device must use lanes 8:9.
   c. When using 1x4 + 1x2 + 1x1, 4 lane device must use lanes 0:3, two lane device must use lanes 8:9, one lane device must use lane 12.

```
CFG [19:8] :RESERVED                1 = NORMAL OPERATION(default)
CFG [7] :PEG DEFER TRAINING         1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB   0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION         11 = 1 X16 (default)   10 = 2 X8    01 = RSVD    00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE         1 = DISABLED(default)                 0 = ENABLED
CFG [3] :RESERVED                   1 = NORMAL OPERATION(default)
CFG [2] :PCIE LANE REVERSAL         1 = NORMAL OPERATION(DEFAULT)         0 = LANES REVERSED
CFG [1] :RESERVED                   1 = NORMAL OPERATION(default)
CFG [0] :STALL RESET SEQUENCE       1 = NORMAL OPERATION(default)         0 = STALL

**ALL CFG PINS DEFAULT TO HIGH WITH 3K INTERNAL PULLUPS UNLESS PULLED LOW ON BOARD.
```

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE	CPU & CHIPSET: CPU Clock/Misc/JTAG/CFG
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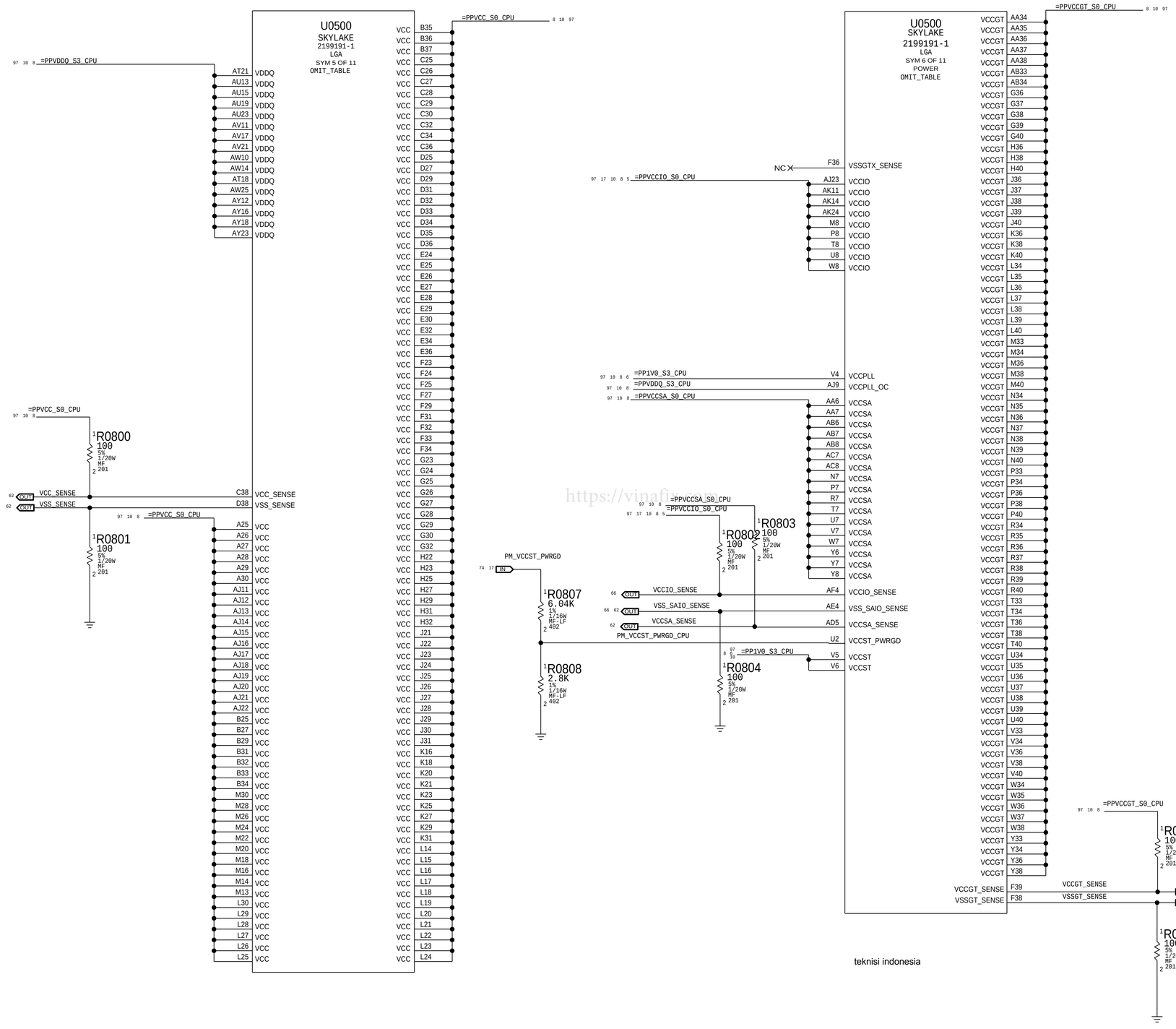

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BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=DORESSLER SYNC_DATE=02/03/2016

PAGE TITLE

CPU & CHIPSET: CPU Power

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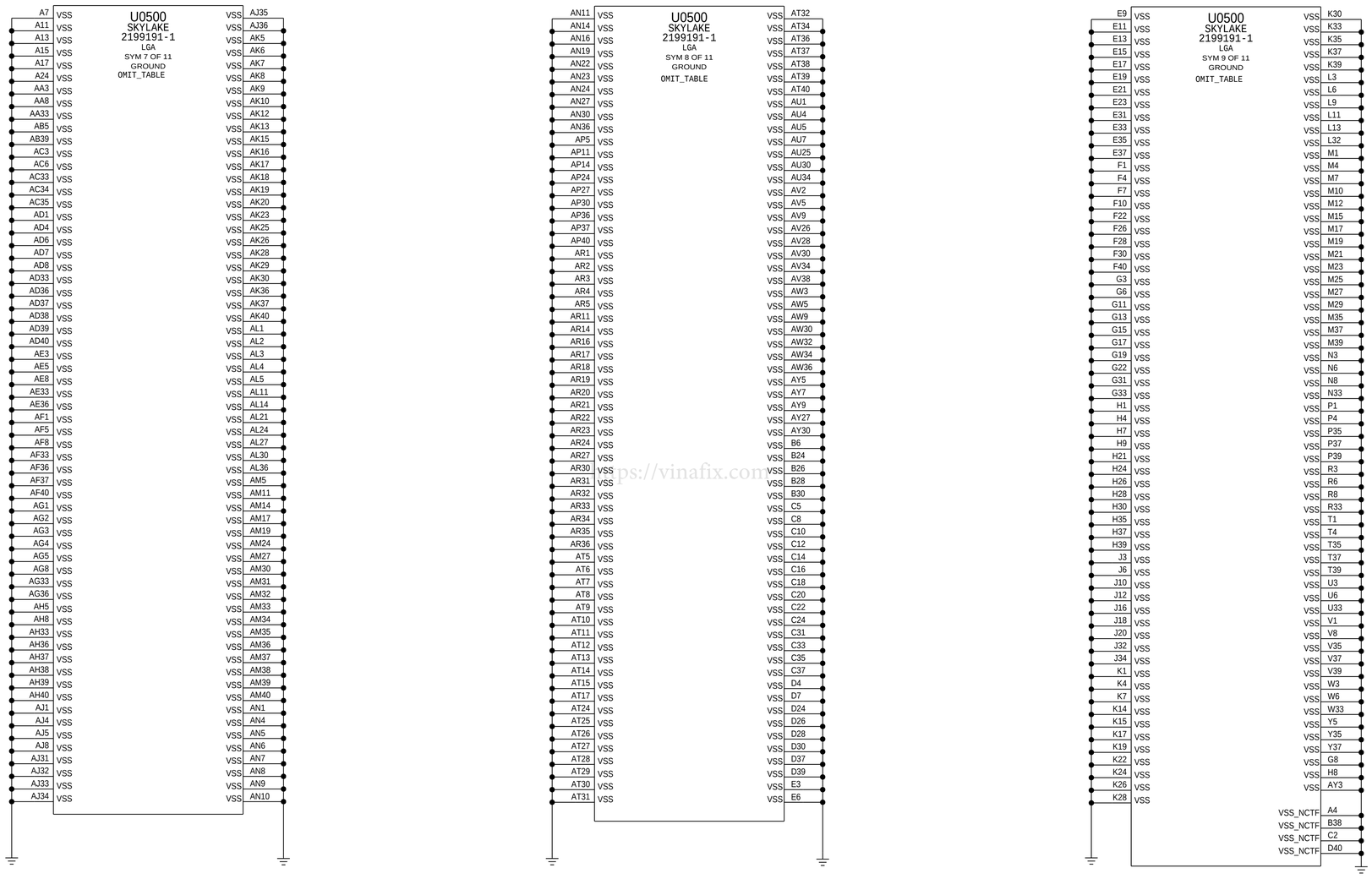

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SYNC_MASTER=DORESSLER SYNC_DATE=02/03/2016

PAGE TITLE

CPU & CHIPSET: CPU Ground

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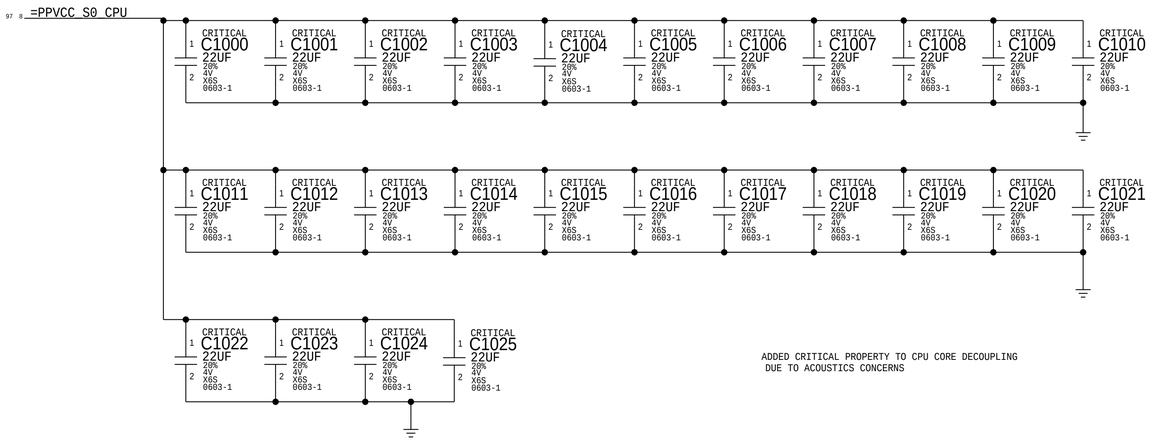
CPU VCORE DECOUPLING

Intel Recommendation:12x 22UF 0805 (top side cavity)
6x 22UF 0603 (top side cavity)
5x 22UF 0805 (top side outside cavity)

Apple Implementation:26x 22UF 0603

Layout Note: These caps should be placed symmetrically on Top and Bottom sides.
BULK CAPS ON CPU VREG PAGE 71



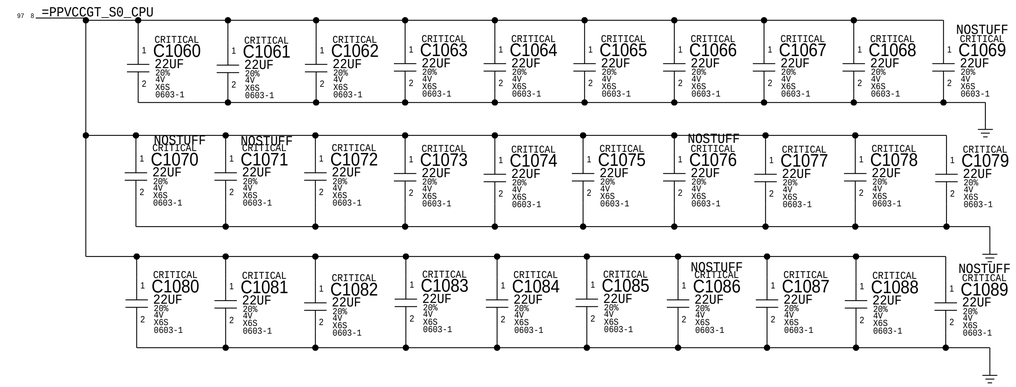
ADDED CRITICAL PROPERTY TO CPU CORE DECOUPLING
DUE TO ACOUSTICS CONCERNS

CPU GT DECOUPLING

INTEL RECOMMENDATION:8X 47UF 0805 (TOP SIDE CAVITY)
4x 47UF 0805 (top side outside cavity)

Apple Implementation: 30x 22uF 0603

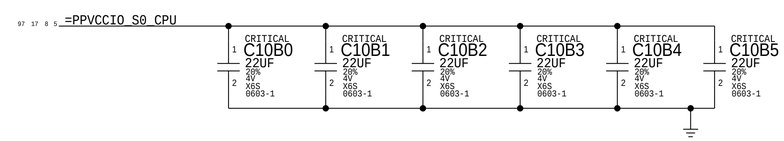
Layout Note: These caps should be placed symmetrically on Top and Bottom sides.



CPU VCCIO DECOUPLING

Intel Recommendation:5x 22UF 0603 (top side cavity)
1x 22UF 0805 (top side cavity)

Apple Implementation:(following Intel recommendation w/ 0603)
Layout Note: These caps should be placed symmetrically on Top and Bottom sides.



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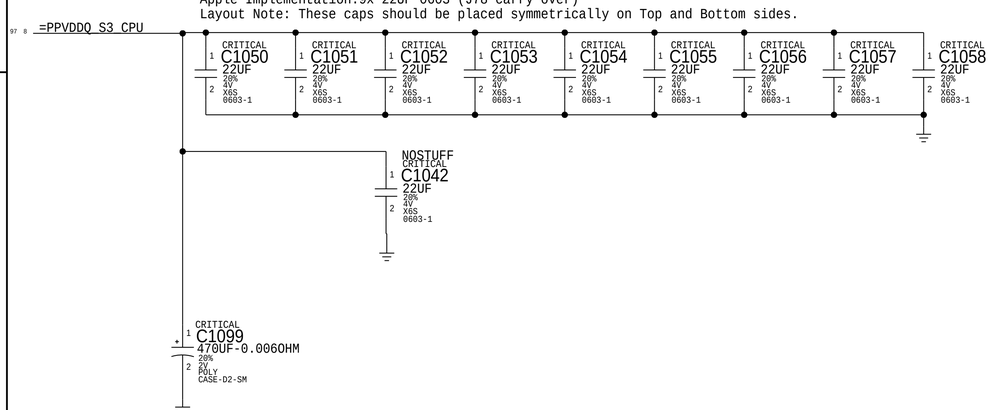
Memory (CPU VCCDDR) DECOUPLING

INTEL RECOMMENDATION:4X 22UF 0603 (TOP SIDE OUTSIDE SOCKET CAP)

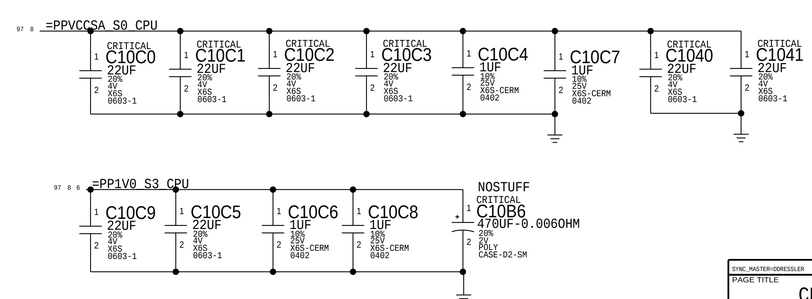
Apple Implementation:9x 22UF 0603 (J78 carry over)
Layout Note: These caps should be placed symmetrically on Top and Bottom sides.



CPU VCCSA / VCCST+VCCPLL DECOUPLING

Intel Recommendation:2x 22UF 0603 near top side cavity

Apple Implementation: VCCST/VCCPLL: 1X 22UF 0603/2X 1UF 0402
Layout Note: These caps should be placed on top side cavity.



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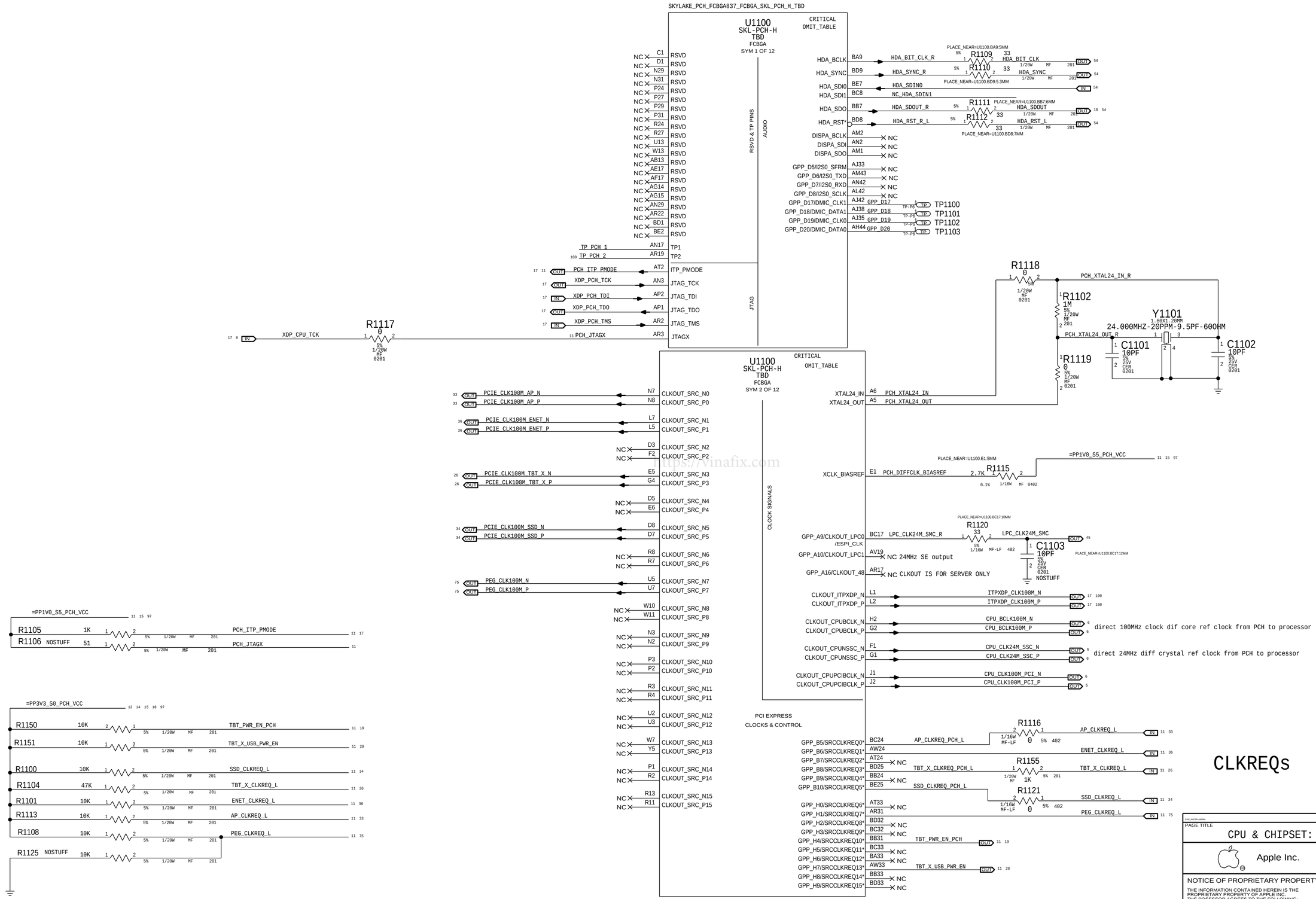

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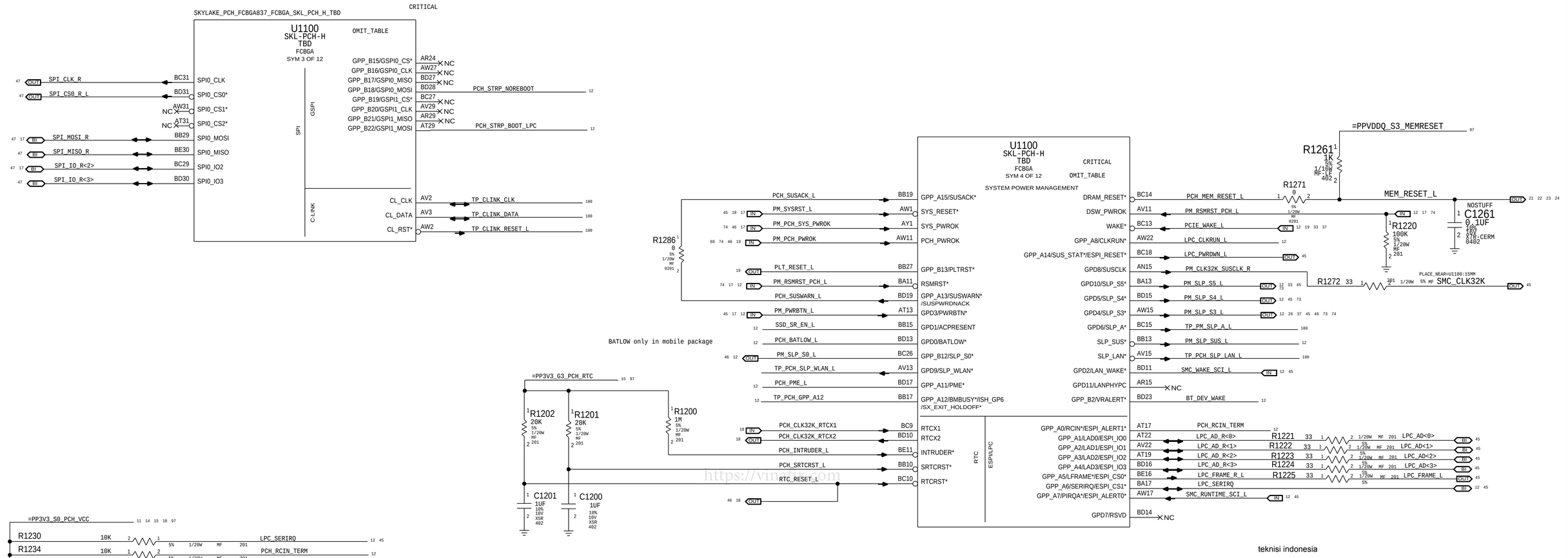

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CPU & CHIPSET: PCH RTC/DMI/PM/CPU_Misc

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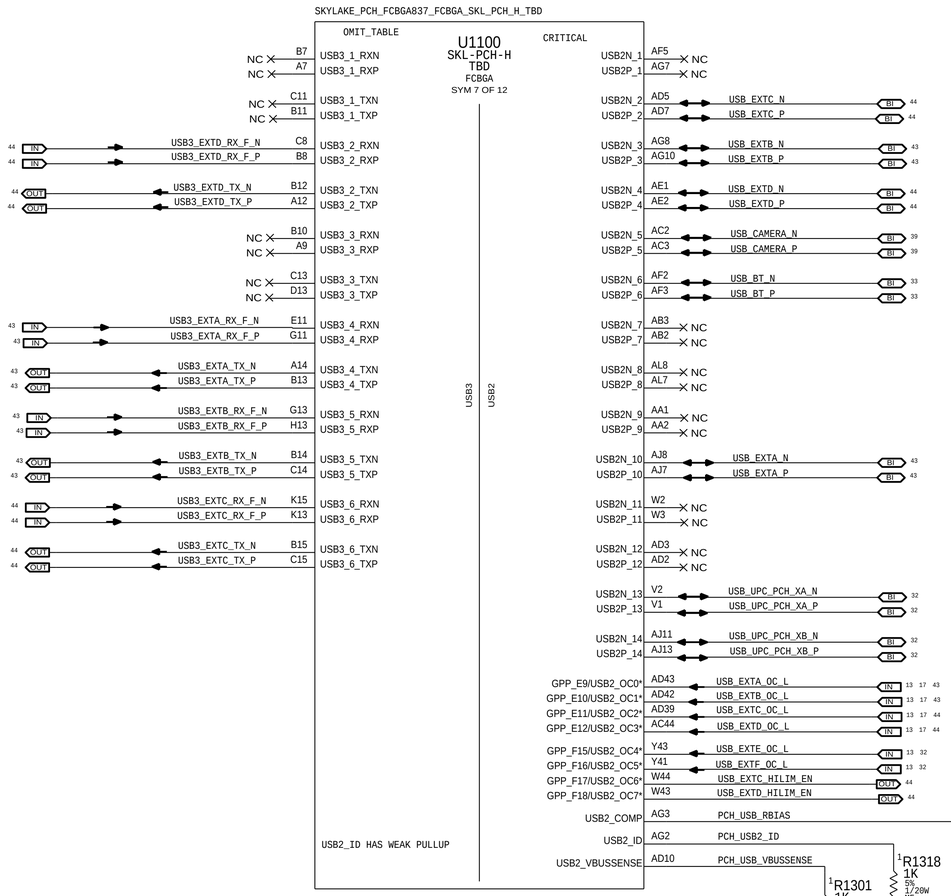

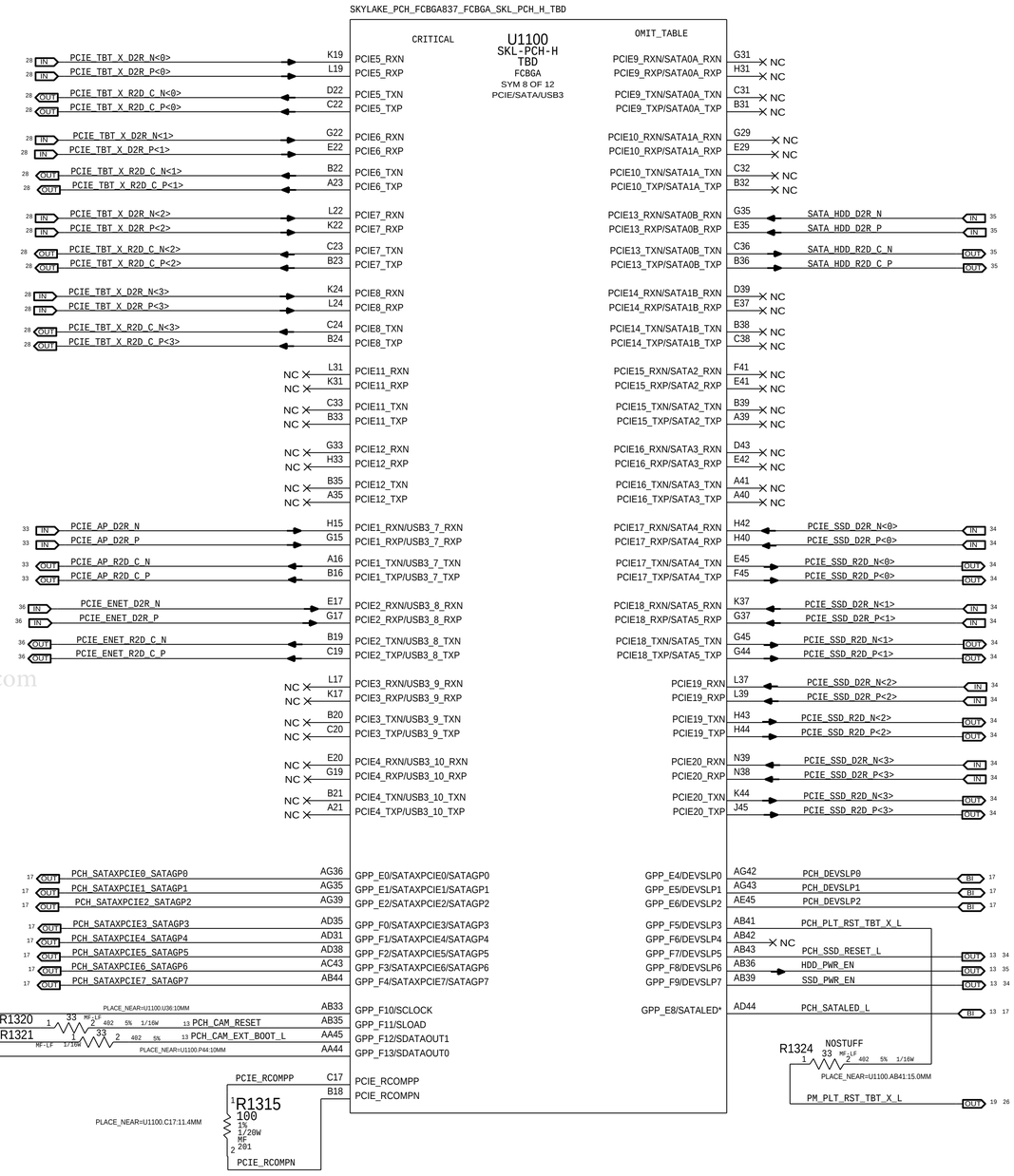

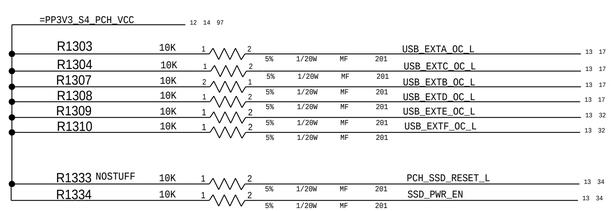

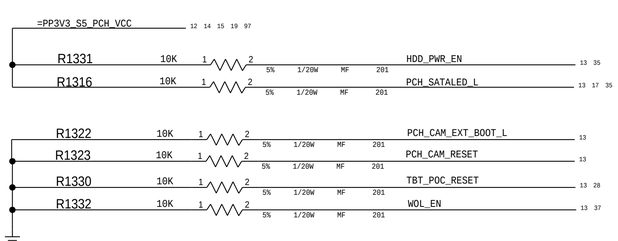

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CPU & CHIPSET: PCH PCI-E/USB

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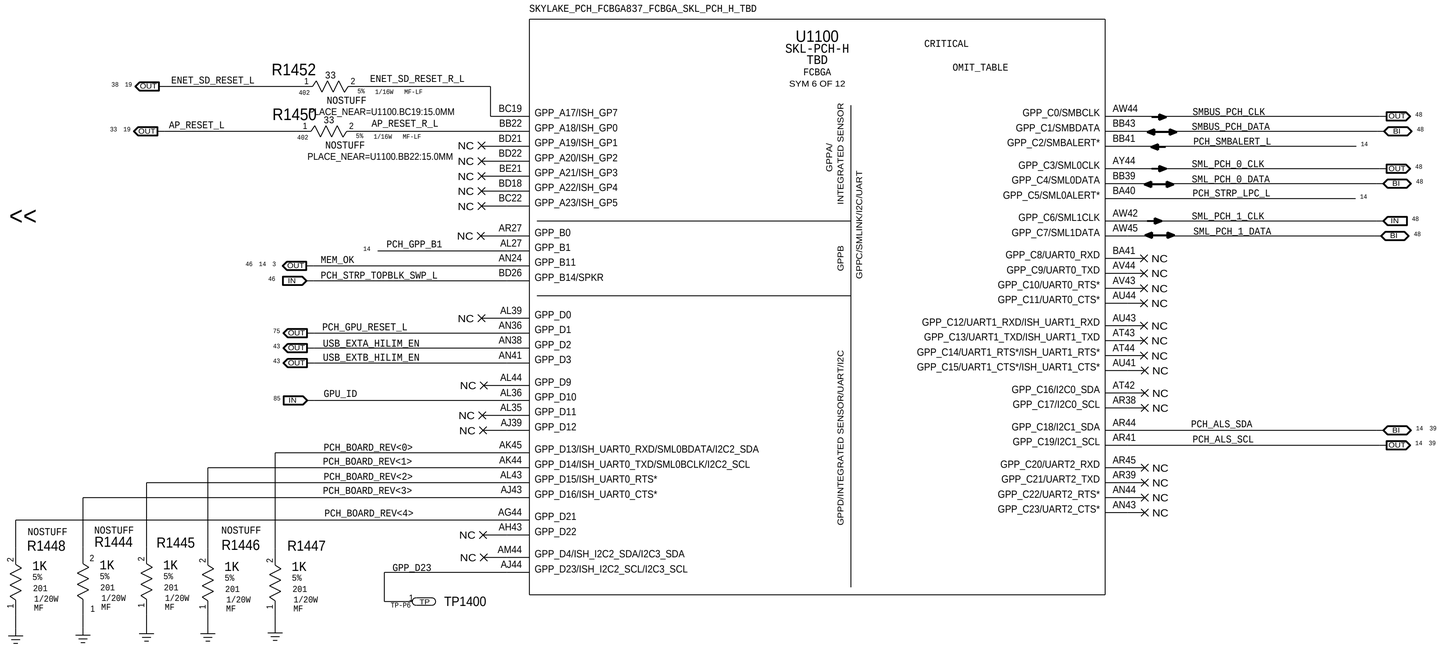
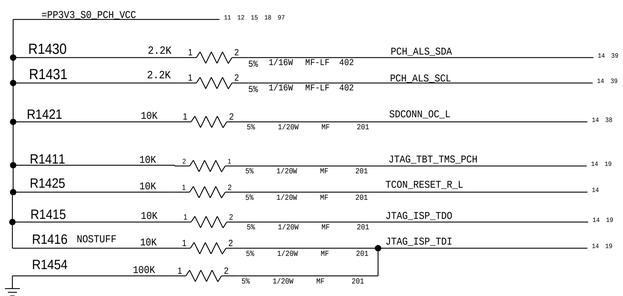
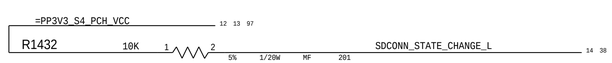
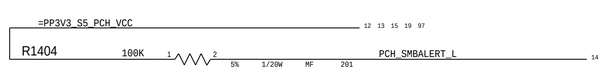
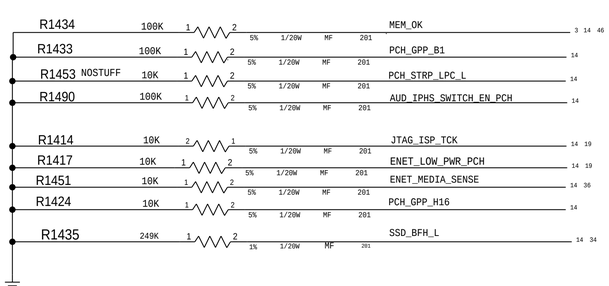
PROTO-1:	11100
PRE-EVT:	11011
EVT:	11010 <<

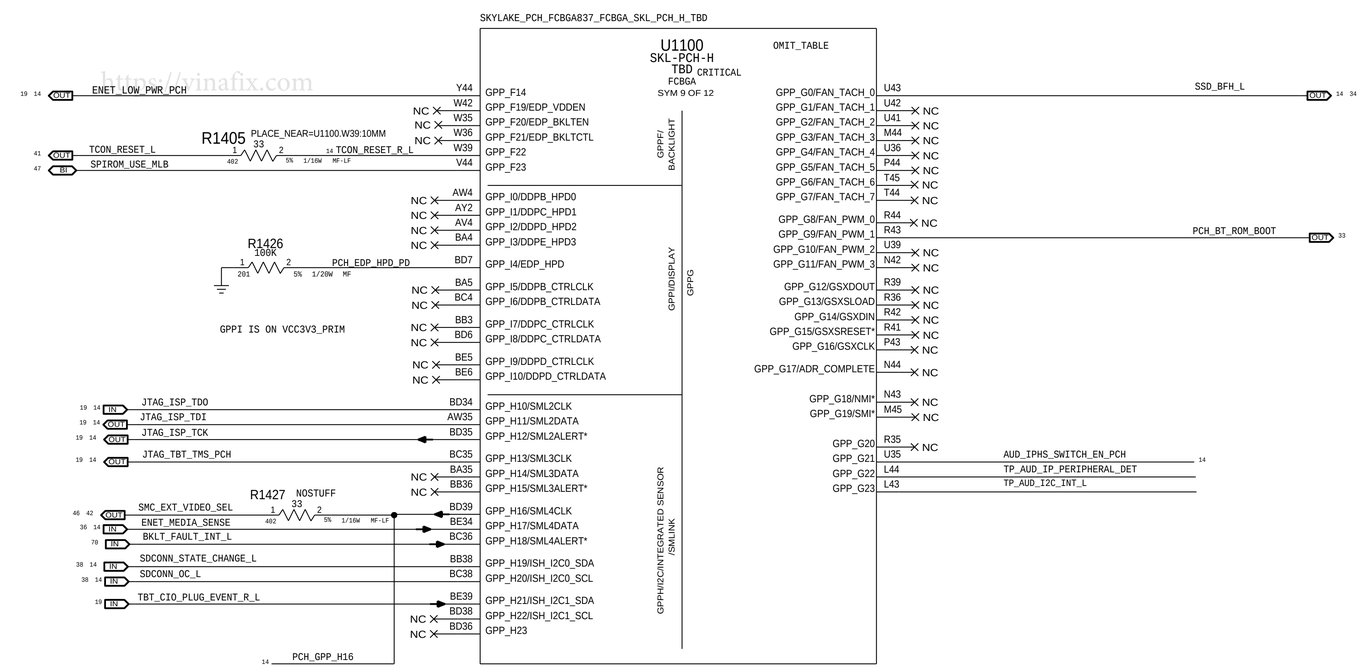












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BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
CPU & CHIPSET: PCH GPIO/Misc

Apple Inc.

DRAWING NUMBER 051-01506
SIZE D
REVISION 5.19.0
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PAGE 14 OF 121
SHEET 14 OF 102

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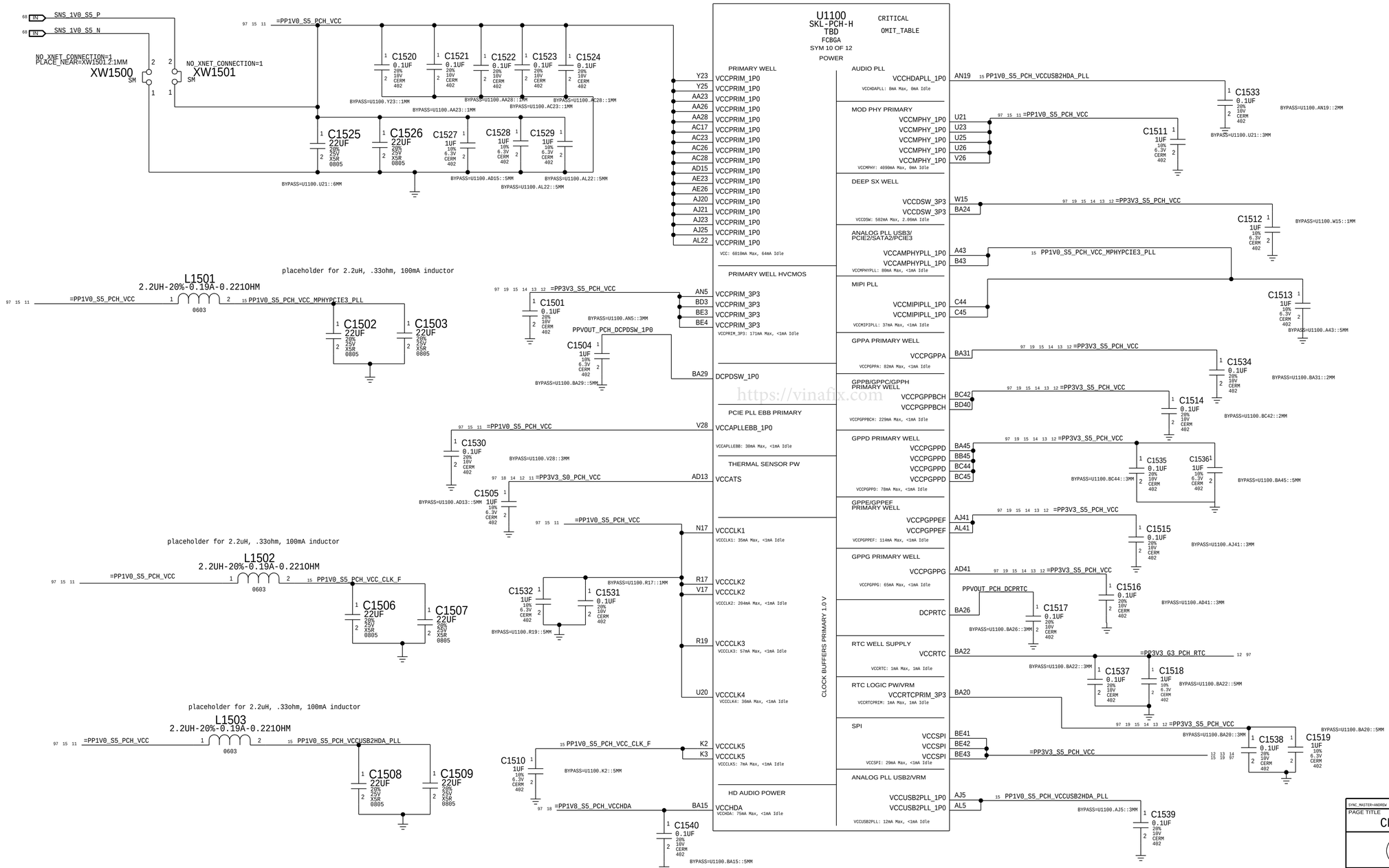
NEED TO ADD 47UF BULK CAPS TO 1.0V AND 3.3V RAIL



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Current data from EDS (doc #546717, Rev 0.7).

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=ANDREW	SYNC_DATE=02/19/2016
PAGE TITLE	CPU & CHIPSET: PCH Power/Decoupling
Apple Inc.	DRAWING NUMBER 051-01506 / SIZE D
	REVISION 5.19.0
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SKYLAKE_PCH_FCBGA837_FCBGA_SKL_PCH_H_TBD

U1100
SKL-PCH-H
TBD
FCBGA
SYM 11 OF 12

CRITICAL

OMIT_TABLE

A2	VSS	VSS	M35
A3	VSS	VSS	M42
A4	VSS	VSS	N4
A18	VSS	VSS	N5
A25	VSS	VSS	N10
A32	VSS	VSS	N15
A37	VSS	VSS	N19
A42	VSS	VSS	N22
A44	VSS	VSS	N24
B1	VSS	VSS	N35
B2	VSS	VSS	N36
B3	VSS	VSS	N41
B6	VSS	VSS	P17
B25	VSS	VSS	P19
B37	VSS	VSS	P22
B40	VSS	VSS	P45
B44	VSS	VSS	R5
B45	VSS	VSS	R10
C2	VSS	VSS	R14
C4	VSS	VSS	R22
C10	VSS	VSS	R29
C28	VSS	VSS	R33
C37	VSS	VSS	R38
C42	VSS	VSS	T1
D10	VSS	VSS	T2
D12	VSS	VSS	T4
D15	VSS	VSS	T42
D16	VSS	VSS	U4
D17	VSS	VSS	U8
D19	VSS	VSS	U10
D21	VSS	VSS	U11
D24	VSS	VSS	U14
D25	VSS	VSS	U15
D27	VSS	VSS	U17
D29	VSS	VSS	U18
D30	VSS	VSS	U28
D31	VSS	VSS	U29
D33	VSS	VSS	U31
D35	VSS	VSS	U32
D36	VSS	VSS	U33
D45	VSS	VSS	U38
E13	VSS	VSS	V3
E15	VSS	VSS	V18
E31	VSS	VSS	V20
E33	VSS	VSS	V21
F8	VSS	VSS	V23
F44	VSS	VSS	V25
G9	VSS	VSS	V29
G42	VSS	VSS	V45
H3	VSS	VSS	W4
H17	VSS	VSS	W8
H19	VSS	VSS	W14
H22	VSS	VSS	W31
H24	VSS	VSS	W32
H27	VSS	VSS	W33
H29	VSS	VSS	W38
H35	VSS	VSS	Y17
J3	VSS	VSS	Y18
J5	VSS	VSS	Y20
J7	VSS	VSS	Y21
J10	VSS	VSS	Y26
J11	VSS	VSS	Y28
J39	VSS	VSS	Y29
K4	VSS	VSS	AA4
K10	VSS	VSS	AA17
K27	VSS	VSS	AA18
K33	VSS	VSS	AA20
K36	VSS	VSS	AA21
K42	VSS	VSS	AA25
K43	VSS	VSS	AA29
L4	VSS	VSS	AA42
L8	VSS	VSS	AB4
L12	VSS	VSS	AB5
L13	VSS	VSS	AB7
L15	VSS	VSS	AB8
L41	VSS	VSS	AB10

SKYLAKE_PCH_FCBGA837_FCBGA_SKL_PCH_H_TBD

U1100
SKL-PCH-H
TBD
FCBGA
SYM 12 OF 12

CRITICAL

OMIT_TABLE

AB11	VSS	VSS	AL32
AB14	VSS	VSS	AL33
AB15	VSS	VSS	AL38
AB31	VSS	VSS	AM15
AB32	VSS	VSS	AM17
AB38	VSS	VSS	AM19
AC1	VSS	VSS	AM22
AC18	VSS	VSS	AM24
AC20	VSS	VSS	AM27
AC21	VSS	VSS	AM29
AC25	VSS	VSS	AM45
AC29	VSS	VSS	AN4
AC45	VSS	VSS	AN7
AD4	VSS	VSS	AN8
AD8	VSS	VSS	AN10
AD11	VSS	VSS	AN11
AD14	VSS	VSS	AN22
AD32	VSS	VSS	AN27
AD33	VSS	VSS	AN31
AD36	VSS	VSS	AN39
AE4	VSS	VSS	AP4
AE18	VSS	VSS	AP11
AE20	VSS	VSS	AR5
AE21	VSS	VSS	AR7
AE25	VSS	VSS	AR9
AE28	VSS	VSS	AR33
AE29	VSS	VSS	AR34
AE42	VSS	VSS	AR42
AF18	VSS	VSS	AT9
AF20	VSS	VSS	AT10
AF21	VSS	VSS	AT15
AF23	VSS	VSS	AT36
AF25	VSS	VSS	AU1
AF26	VSS	VSS	AU7
AF28	VSS	VSS	AU35
AF29	VSS	VSS	AU36
AG4	VSS	VSS	AU39
AG11	VSS	VSS	AU45
AG13	VSS	VSS	AV6
AG31	VSS	VSS	AV17
AG32	VSS	VSS	AV24
AG33	VSS	VSS	AV27
AG38	VSS	VSS	AV31
AH1	VSS	VSS	AV33
AH17	VSS	VSS	AW9
AH18	VSS	VSS	AW13
AH20	VSS	VSS	AW19
AH21	VSS	VSS	AW29
AH23	VSS	VSS	AW37
AH25	VSS	VSS	AY38
AH26	VSS	VSS	AY45
AH28	VSS	VSS	BA1
AH29	VSS	VSS	BB1
AH45	VSS	VSS	BB11
AJ10	VSS	VSS	BB16
AJ14	VSS	VSS	BB21
AJ15	VSS	VSS	BB25
AJ17	VSS	VSS	BB30
AJ18	VSS	VSS	BB34
AJ26	VSS	VSS	BC1
AJ28	VSS	VSS	BC2
AJ29	VSS	VSS	BD2
AJ31	VSS	VSS	BD43
AJ32	VSS	VSS	BD44
AJ36	VSS	VSS	BD45
AK4	VSS	VSS	BE9
AK42	VSS	VSS	BE14
AL4	VSS	VSS	BE18
AL10	VSS	VSS	BE23
AL11	VSS	VSS	BE28
AL13	VSS	VSS	BE32
AL17	VSS	VSS	BE37
AL19	VSS	VSS	BE40
AL24	VSS	VSS	BE44
AL29	VSS		

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BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=kchooMLB SYNC_DATE=10/30/2015

PAGE TITLE
CPU & CHIPSET: PCH Grounds

Apple Inc.

DRAWING NUMBER 051-01506
SIZE D
REVISION 5.19.0
BRANCH
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SHEET 16 OF 102

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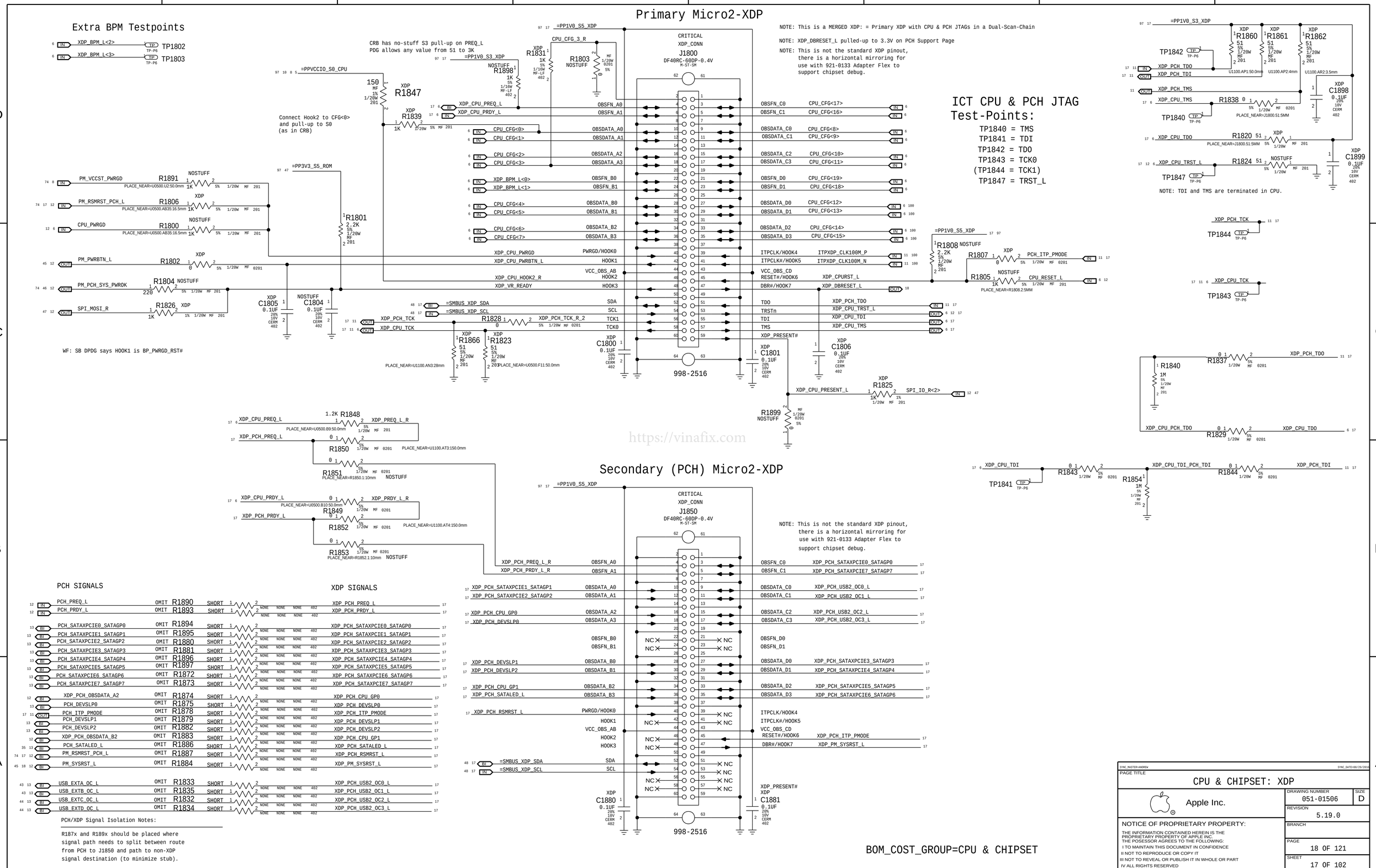
Primary Micro2-XDP
Extra BPM Testpoints
TP1802
TP1803
CRB has no-stuff S3 pull-up on PREQ_L
PDG allows any value from 51 to 3K
Connect Hook2 to CFG<0>
and pull-up to S0
(as in CRB)
CRITICAL
XDP_CONN
J1800
DF40RC-60DP-0.4V
M-ST-SM
998-2516
NOTE: This is a MERGED XDP: = Primary XDP with CPU & PCH JTAGs in a Dual-Scan-Chain
NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page
NOTE: This is not the standard XDP pinout,
there is a horizontal mirroring for
use with 921-0133 Adapter Flex to
support chipset debug.
ICT CPU & PCH JTAG
Test-Points:
TP1840 = TMS
TP1841 = TDI
TP1842 = TDO
TP1843 = TCK0
(TP1844 = TCK1)
TP1847 = TRST_L
NOTE: TDI and TMS are terminated in CPU.
WF: SB DPDG says HOOK1 is BP_PWRGD_RST#
https://vinafix.com
Secondary (PCH) Micro2-XDP
CRITICAL
XDP_CONN
J1850
DF40RC-60DP-0.4V
M-ST-SM
998-2516
NOTE: This is not the standard XDP pinout,
there is a horizontal mirroring for
use with 921-0133 Adapter Flex to
support chipset debug.
PCH SIGNALS
XDP SIGNALS
PCH/XDP Signal Isolation Notes:
R187x and R189x should be placed where
signal path needs to split between route
from PCH to J1850 and path to non-XDP
signal destination (to minimize stub).
BOM_COST_GROUP=CPU & CHIPSET
CPU & CHIPSET: XDP
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SIZE D
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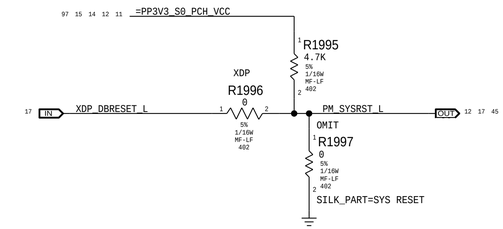
PCH Reset Button



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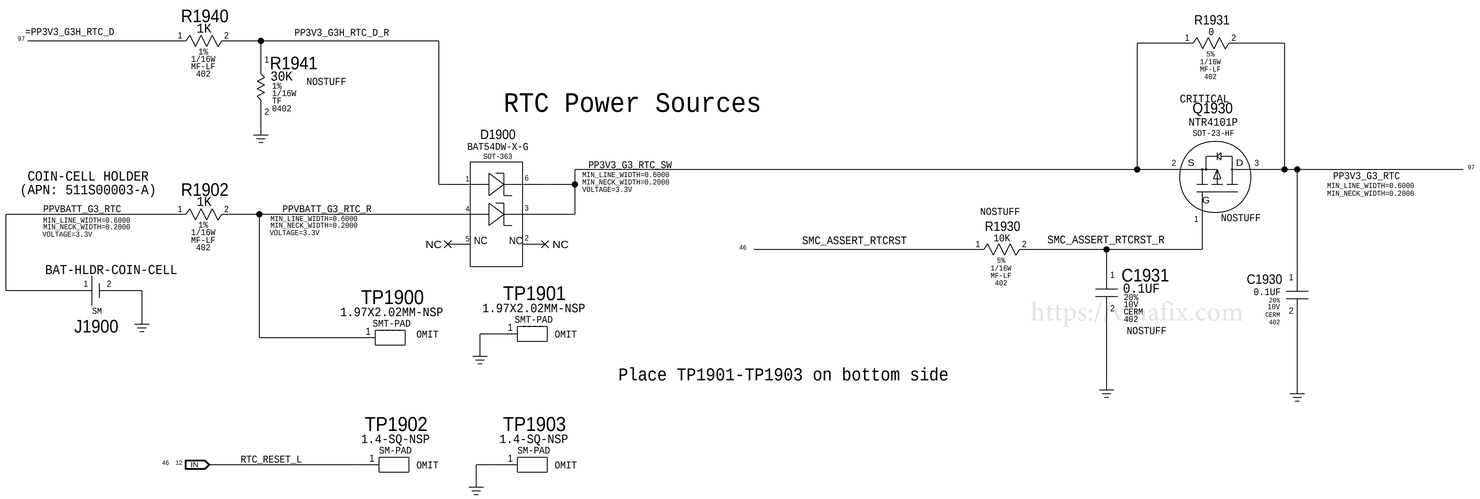
RTC Power Sources



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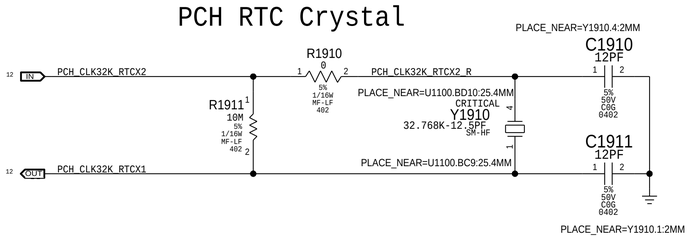
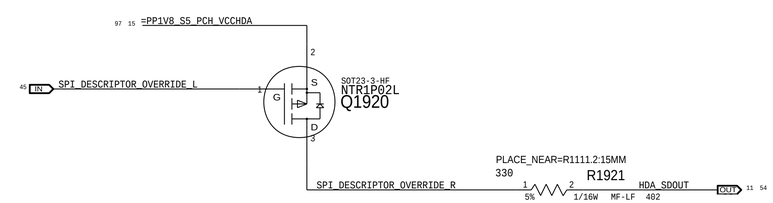
Place TP1901-TP1903 on bottom side

PCH RTC Crystal



PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.



BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE	CPU & CHIPSET: Chipset Support
Apple Inc.	DRAWING NUMBER 051-01506 / SIZE D
	REVISION 5.19.0
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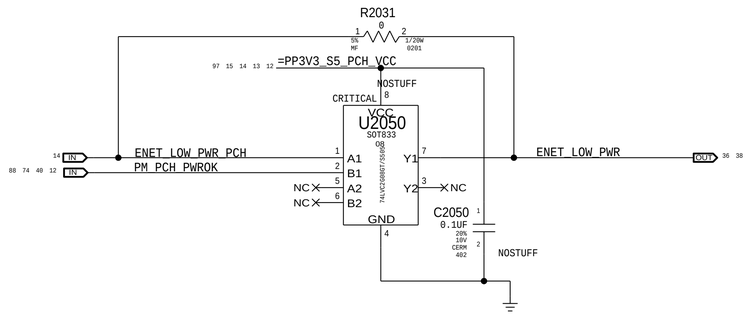
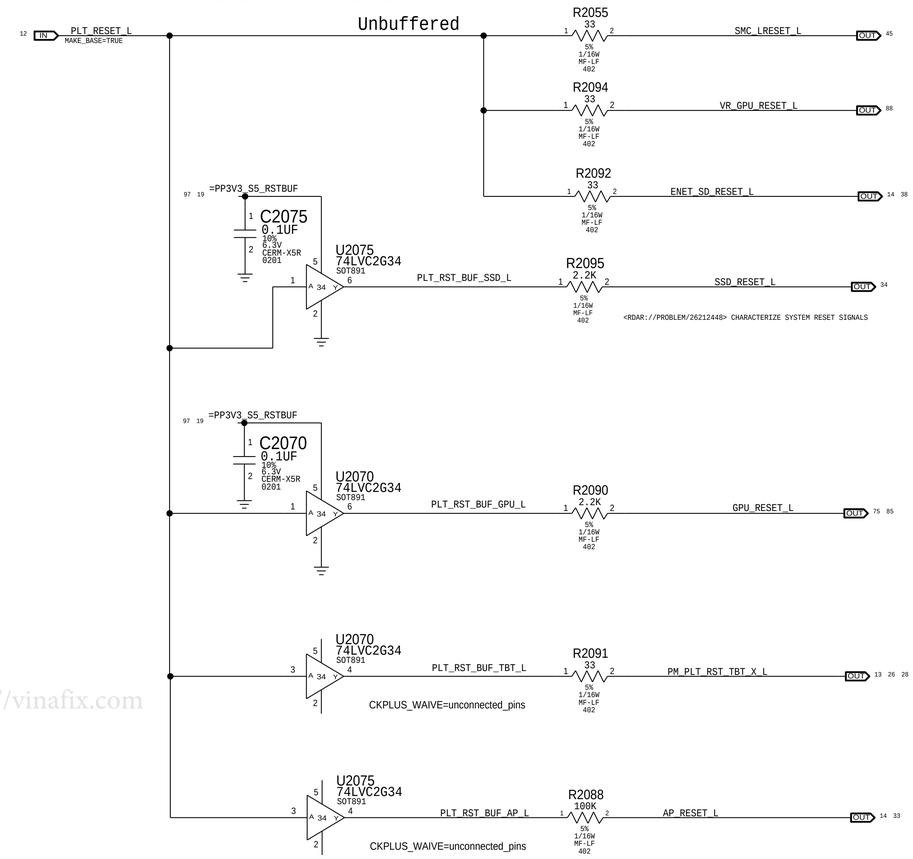
GPIO Glitch Prevention



Platform Reset Connections



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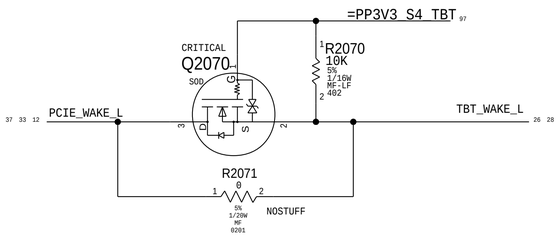

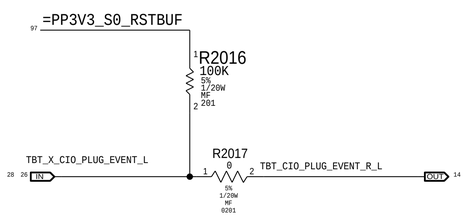

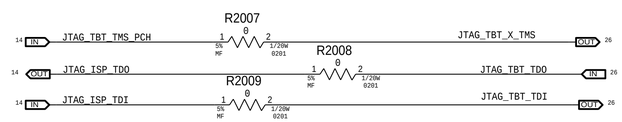

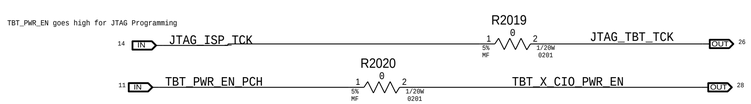

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=HAMCK	SYNC_DATE=06/22/2010
PAGE TITLE	CPU & CHIPSET: Project Chipset Support
Apple Inc.	DRAWING NUMBER 051-01506 / SIZE D
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	SHEET 19 OF 102

**Removed DQ VREF dividers from DDR3L
**DDR4 DIMM Internal DQ Vref

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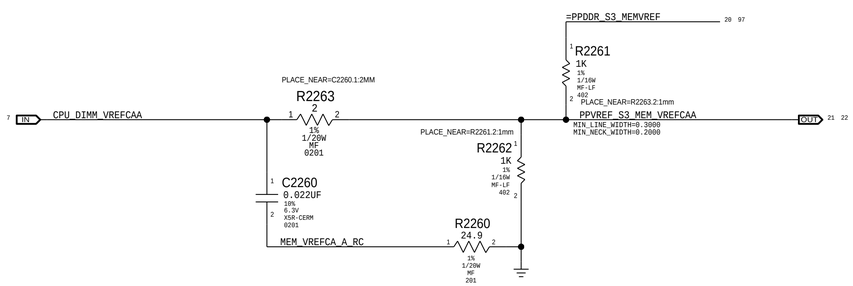
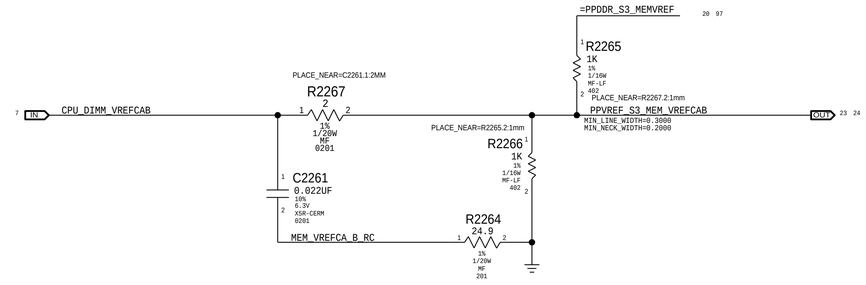
VRef Dividers



VRef Dividers



BOM_COST_GROUP=DRAM

PAGE TITLE	DRAM:VREF/VTT EN
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	SHEET 20 OF 102

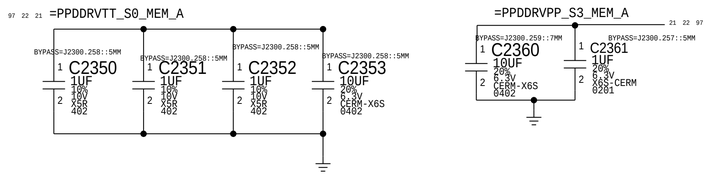
Page Notes

Power aliases required by this page:
- =PPDDRVPP_S3_MEM_A
- =PPVDDQ_S3_MEM_A
- =PPDDRVTT_S0_MEM_A
- =PP3V3_S0_MEM_A_SPD (2.5 - 3.3V)

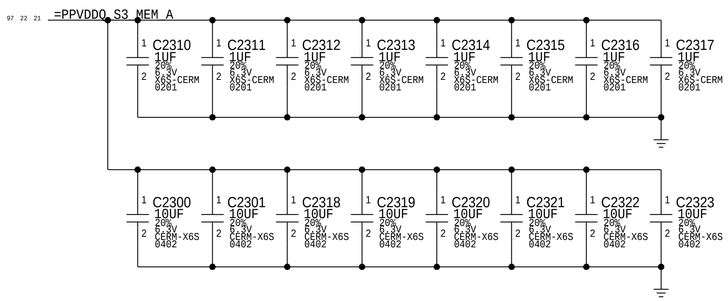
Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

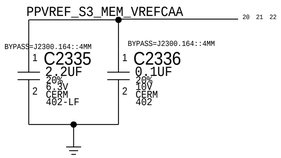
BOM options provided by this page:
(NONE)

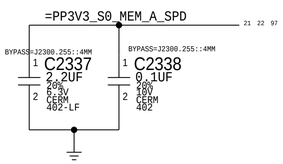
P/N: 516S00204

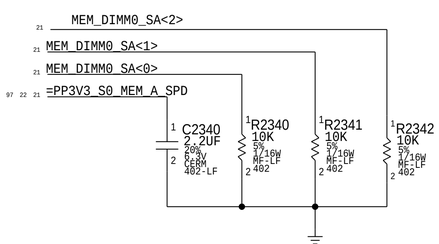


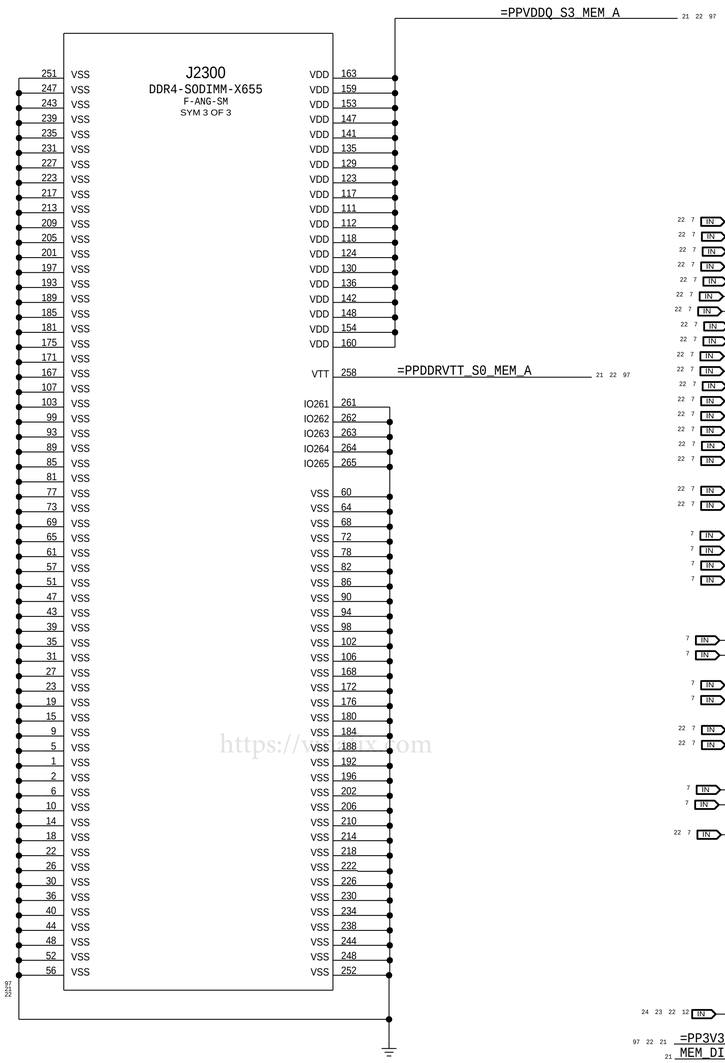
DDR4 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

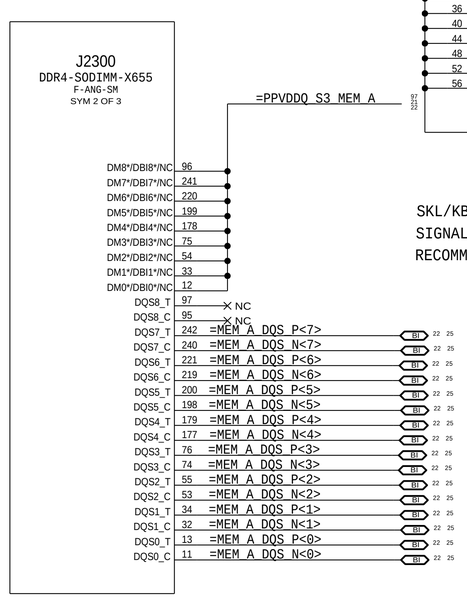




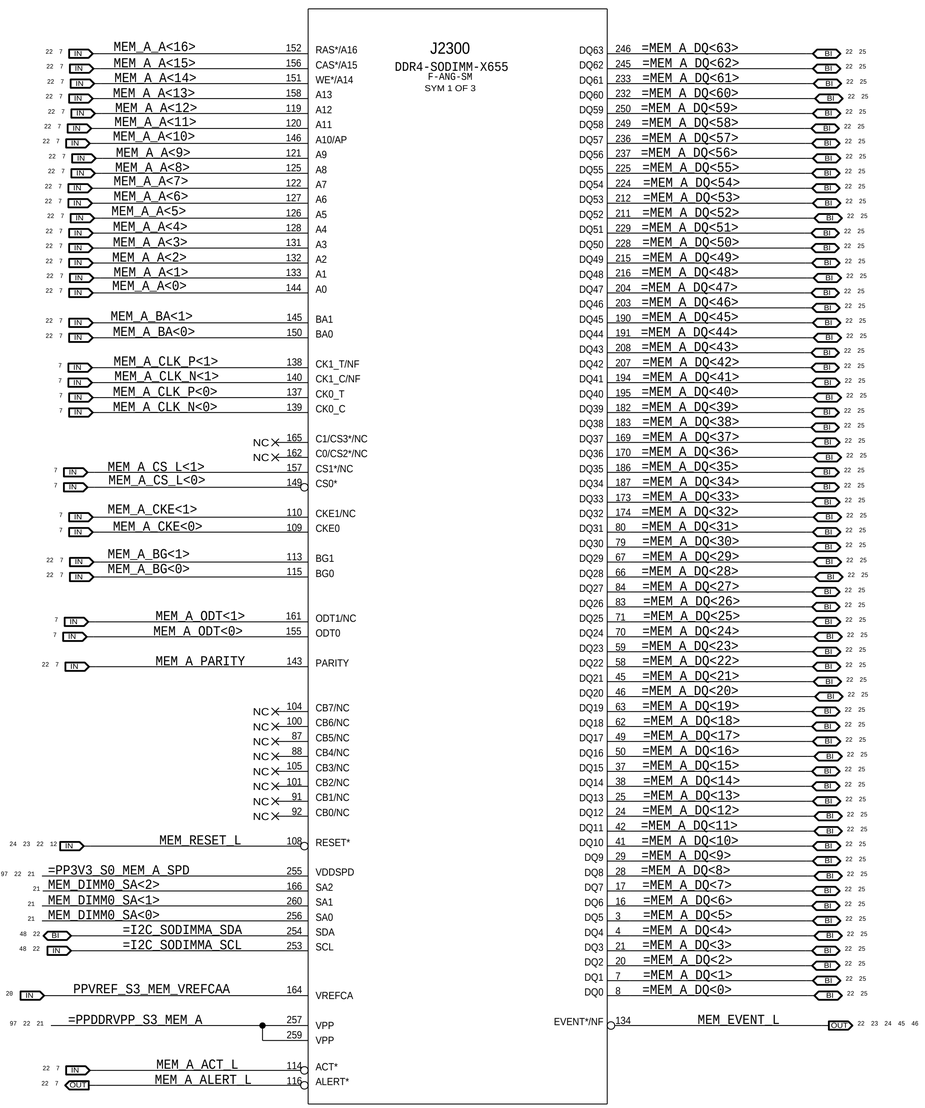








SKL/KBL DOES NOT SUPPORT DM (DATAMASK)
SIGNAL IS ACTIVE LOW FOR DDR4
RECOMMENDED TO PULL TO VDDQ TO DISABLE FUNCITON



BOM_COST_GROUP=DRAM

PAGE TITLE	DRAM: SO-DIMM Connector A Slot0
Apple Inc.	DRAWING NUMBER 051-01506 SIZE D
	REVISION 5.19.0
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	SHEET 21 OF 102

Page Notes

Power aliases required by this page:
- =PPDDRVPP_S3_MEM_A
- =PPVDDQ_S3_MEM_A
- =PPDDRVTT_S0_MEM_A
- =PP3V3_S0_MEM_A_SPD (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

P/N: 516S00204

=PPDDRVTT_S0_MEM_A

=PPDDRVPP_S3_MEM_A

C2450 1UF 10% 10V X5R 402 — C2451 1UF 10% 10V X5R 402 — C2452 1UF 10% 10V X5R 402 — C2453 10UF 20% 6.3V CERM-X6S 0402

C2460 10UF 20% 6.3V CERM-X6S 0402 — C2461 1UF 20% 6.3V X6S-CERM 0201

DDR4 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

=PPVDDQ_S3_MEM_A

C2410 C2411 C2412 C2413 C2414 C2415 C2416 C2417 1UF 20% 6.3V X6S-CERM 0201

C2400 C2401 C2418 C2419 C2420 C2421 C2422 C2423 10UF 20% 6.3V CERM-X6S 0402

PPVREF_S3_MEM_VREFCAA

C2435 2.2UF 20% 6.3V CERM 402-LF — C2436 0.1UF 10% 10V CERM 402

teknisi indonesia

=PP3V3_S0_MEM_A_SPD

C2437 2.2UF 20% 6.3V CERM 402-LF — C2438 0.1UF 20% 10V CERM 402

=PP3V3_S0_MEM_A_SPD — R2440 10K 5% 1/16W MF-LF 402 — MEM_DIMM1_SA<0>

MEM_DIMM1_SA<2>
MEM_DIMM1_SA<1>
=PP3V3_S0_MEM_A_SPD
C2440 2.2UF 20% 6.3V CERM 402-LF — R2441 10K 5% 1/16W MF-LF 402 — R2442 10K 5% 1/16W MF-LF 402

J2400 DDR4-SODIMM-X655 F-ANG-SM SYM 3 OF 3

Pin	Signal	Pin	Signal
251	VSS	163	VDD
247	VSS	159	VDD
243	VSS	153	VDD
239	VSS	147	VDD
235	VSS	141	VDD
231	VSS	135	VDD
227	VSS	129	VDD
223	VSS	123	VDD
217	VSS	117	VDD
213	VSS	111	VDD
209	VSS	112	VDD
205	VSS	118	VDD
201	VSS	124	VDD
197	VSS	130	VDD
193	VSS	136	VDD
189	VSS	142	VDD
185	VSS	148	VDD
181	VSS	154	VDD
175	VSS	160	VDD
171	VSS		
167	VSS	258	VTT
107	VSS		
103	VSS	261	IO261
99	VSS	262	IO262
93	VSS	263	IO263
89	VSS	264	IO264
85	VSS	265	IO265
81	VSS		
77	VSS	60	VSS
73	VSS	64	VSS
69	VSS	68	VSS
65	VSS	72	VSS
61	VSS	78	VSS
57	VSS	82	VSS
51	VSS	86	VSS
47	VSS	90	VSS
43	VSS	94	VSS
39	VSS	98	VSS
35	VSS	102	VSS
31	VSS	106	VSS
27	VSS	168	VSS
23	VSS	172	VSS
19	VSS	176	VSS
15	VSS	180	VSS
9	VSS	184	VSS
5	VSS	188	VSS
1	VSS	192	VSS
2	VSS	196	VSS
6	VSS	202	VSS
10	VSS	206	VSS
14	VSS	210	VSS
18	VSS	214	VSS
22	VSS	218	VSS
26	VSS	222	VSS
30	VSS	226	VSS
36	VSS	230	VSS
40	VSS	234	VSS
44	VSS	238	VSS
48	VSS	244	VSS
52	VSS	248	VSS
56	VSS	252	VSS

J2400 DDR4-SODIMM-X655 F-ANG-SM SYM 2 OF 3

=PPVDDQ_S3_MEM_A

Pin	Signal	Net
96	DM8*/DBI8*/NC	
241	DM7*/DBI7*/NC	
220	DM6*/DBI6*/NC	
199	DM5*/DBI5*/NC	
178	DM4*/DBI4*/NC	
75	DM3*/DBI3*/NC	
54	DM2*/DBI2*/NC	
33	DM1*/DBI1*/NC	
12	DM0*/DBI0*/NC	
97	DQS8_T	NC
95	DQS8_C	NC
242	DQS7_T	=MEM_A_DQS_P<7>
240	DQS7_C	=MEM_A_DQS_N<7>
221	DQS6_T	=MEM_A_DQS_P<6>
219	DQS6_C	=MEM_A_DQS_N<6>
200	DQS5_T	=MEM_A_DQS_P<5>
198	DQS5_C	=MEM_A_DQS_N<5>
179	DQS4_T	=MEM_A_DQS_P<4>
177	DQS4_C	=MEM_A_DQS_N<4>
76	DQS3_T	=MEM_A_DQS_P<3>
74	DQS3_C	=MEM_A_DQS_N<3>
55	DQS2_T	=MEM_A_DQS_P<2>
53	DQS2_C	=MEM_A_DQS_N<2>
34	DQS1_T	=MEM_A_DQS_P<1>
32	DQS1_C	=MEM_A_DQS_N<1>
13	DQS0_T	=MEM_A_DQS_P<0>
11	DQS0_C	=MEM_A_DQS_N<0>

SKL/KBL DOES NOT SUPPORT DM (DATAMASK)
SIGNAL IS ACTIVE LOW FOR DDR4
RECOMMENDED TO PULL TO VDDQ TO DISABLE FUNCITON

J2400 DDR4-SODIMM-X655 F-ANG-SM SYM 1 OF 3

Pin	Signal	Net
152	RAS*/A16	MEM_A_A<16>
156	CAS*/A15	MEM_A_A<15>
151	WE*/A14	MEM_A_A<14>
158	A13	MEM_A_A<13>
119	A12	MEM_A_A<12>
120	A11	MEM_A_A<11>
146	A10/AP	MEM_A_A<10>
121	A9	MEM_A_A<9>
125	A8	MEM_A_A<8>
122	A7	MEM_A_A<7>
127	A6	MEM_A_A<6>
126	A5	MEM_A_A<5>
128	A4	MEM_A_A<4>
131	A3	MEM_A_A<3>
132	A2	MEM_A_A<2>
133	A1	MEM_A_A<1>
144	A0	MEM_A_A<0>
145	BA1	MEM_A_BA<1>
150	BA0	MEM_A_BA<0>
138	CK1_T/NF	MEM_A_CLK_P<3>
140	CK1_C/NF	MEM_A_CLK_N<3>
137	CK0_T	MEM_A_CLK_P<2>
139	CK0_C	MEM_A_CLK_N<2>
165	C1/CS3*/NC	NC
162	C0/CS2*/NC	NC
157	CS1*/NC	MEM_A_CS_L<3>
149	CS0*	MEM_A_CS_L<2>
110	CKE1/NC	MEM_A_CKE<3>
109	CKE0	MEM_A_CKE<2>
113	BG1	MEM_A_BG<1>
115	BG0	MEM_A_BG<0>
161	ODT1/NC	MEM_A_ODT<3>
155	ODT0	MEM_A_ODT<2>
143	PARITY	MEM_A_PARITY
104	CB7/NC	NC
100	CB6/NC	NC
87	CB5/NC	NC
88	CB4/NC	NC
105	CB3/NC	NC
101	CB2/NC	NC
91	CB1/NC	NC
92	CB0/NC	NC
108	RESET*	MEM_RESET_L
255	VDDSPD	=PP3V3_S0_MEM_A_SPD
166	SA2	MEM_DIMM1_SA<2>
260	SA1	MEM_DIMM1_SA<1>
256	SA0	MEM_DIMM1_SA<0>
254	SDA	=I2C_SODIMMA_SDA
253	SCL	=I2C_SODIMMA_SCL
164	VREFCA	PPVREF_S3_MEM_VREFCAA
257	VPP	=PPDDRVPP_S3_MEM_A
259	VPP	
114	ACT*	MEM_A_ACT_L
116	ALERT*	MEM_A_ALERT_L

Pin	Signal	Net
246	DQ63	=MEM_A_DQ<63>
245	DQ62	=MEM_A_DQ<62>
233	DQ61	=MEM_A_DQ<61>
232	DQ60	=MEM_A_DQ<60>
250	DQ59	=MEM_A_DQ<59>
249	DQ58	=MEM_A_DQ<58>
236	DQ57	=MEM_A_DQ<57>
237	DQ56	=MEM_A_DQ<56>
225	DQ55	=MEM_A_DQ<55>
224	DQ54	=MEM_A_DQ<54>
212	DQ53	=MEM_A_DQ<53>
211	DQ52	=MEM_A_DQ<52>
229	DQ51	=MEM_A_DQ<51>
228	DQ50	=MEM_A_DQ<50>
215	DQ49	=MEM_A_DQ<49>
216	DQ48	=MEM_A_DQ<48>
204	DQ47	=MEM_A_DQ<47>
203	DQ46	=MEM_A_DQ<46>
190	DQ45	=MEM_A_DQ<45>
191	DQ44	=MEM_A_DQ<44>
208	DQ43	=MEM_A_DQ<43>
207	DQ42	=MEM_A_DQ<42>
194	DQ41	=MEM_A_DQ<41>
195	DQ40	=MEM_A_DQ<40>
182	DQ39	=MEM_A_DQ<39>
183	DQ38	=MEM_A_DQ<38>
169	DQ37	=MEM_A_DQ<37>
170	DQ36	=MEM_A_DQ<36>
186	DQ35	=MEM_A_DQ<35>
187	DQ34	=MEM_A_DQ<34>
173	DQ33	=MEM_A_DQ<33>
174	DQ32	=MEM_A_DQ<32>
80	DQ31	=MEM_A_DQ<31>
79	DQ30	=MEM_A_DQ<30>
67	DQ29	=MEM_A_DQ<29>
66	DQ28	=MEM_A_DQ<28>
84	DQ27	=MEM_A_DQ<27>
83	DQ26	=MEM_A_DQ<26>
71	DQ25	=MEM_A_DQ<25>
70	DQ24	=MEM_A_DQ<24>
59	DQ23	=MEM_A_DQ<23>
58	DQ22	=MEM_A_DQ<22>
45	DQ21	=MEM_A_DQ<21>
46	DQ20	=MEM_A_DQ<20>
63	DQ19	=MEM_A_DQ<19>
62	DQ18	=MEM_A_DQ<18>
49	DQ17	=MEM_A_DQ<17>
50	DQ16	=MEM_A_DQ<16>
37	DQ15	=MEM_A_DQ<15>
38	DQ14	=MEM_A_DQ<14>
25	DQ13	=MEM_A_DQ<13>
24	DQ12	=MEM_A_DQ<12>
42	DQ11	=MEM_A_DQ<11>
41	DQ10	=MEM_A_DQ<10>
29	DQ9	=MEM_A_DQ<9>
28	DQ8	=MEM_A_DQ<8>
17	DQ7	=MEM_A_DQ<7>
16	DQ6	=MEM_A_DQ<6>
3	DQ5	=MEM_A_DQ<5>
4	DQ4	=MEM_A_DQ<4>
21	DQ3	=MEM_A_DQ<3>
20	DQ2	=MEM_A_DQ<2>
7	DQ1	=MEM_A_DQ<1>
8	DQ0	=MEM_A_DQ<0>
134	EVENT*/NF	MEM_EVENT_L

BOM_COST_GROUP=DRAM

PAGE TITLE: DRAM: SO-DIMM Connector A Slot1

Apple Inc.

DRAWING NUMBER: 051-01506 SIZE: D
REVISION: 5.19.0
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PAGE: 24 OF 121
SHEET: 22 OF 102

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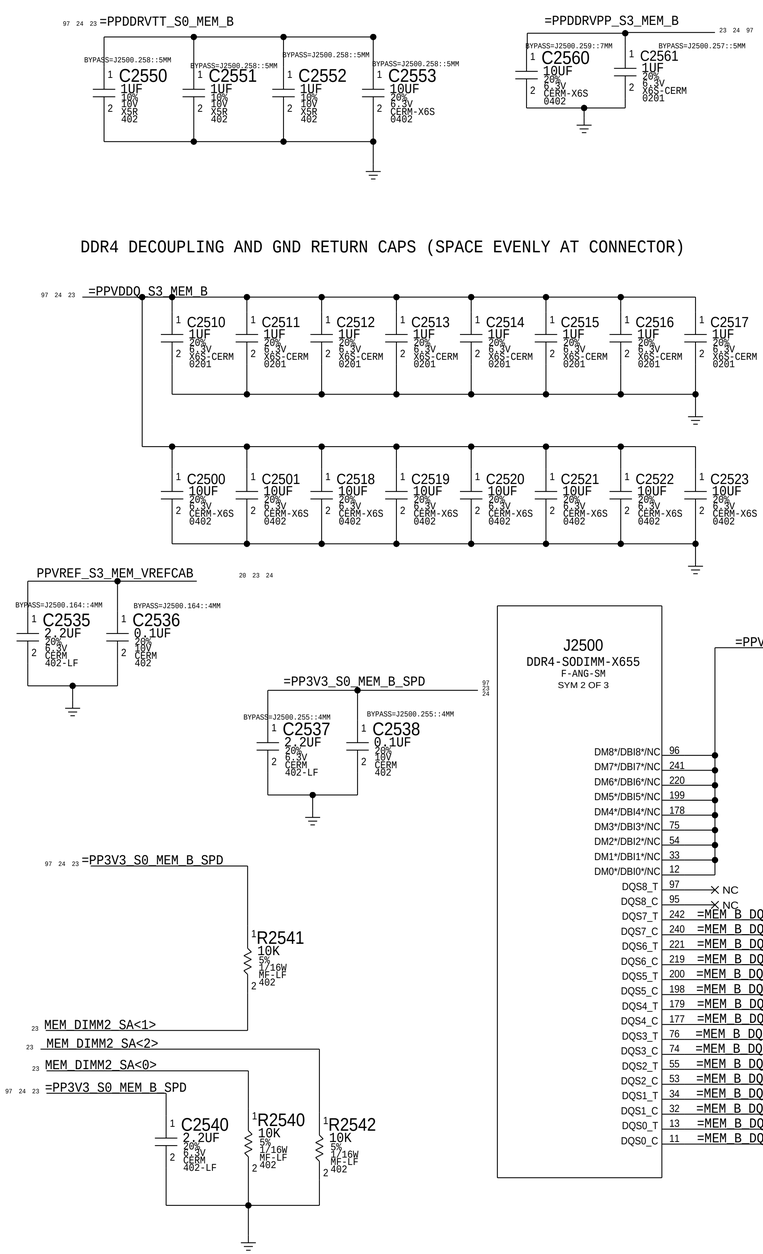
Page Notes

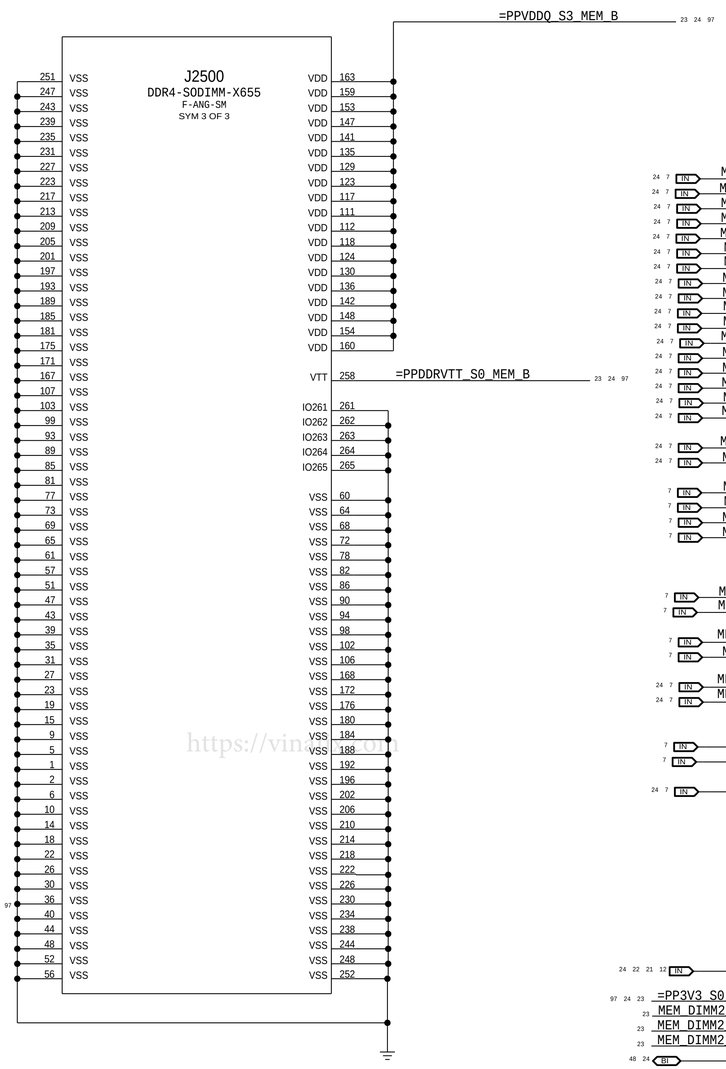
Power aliases required by this page:
- =PPDDRVPP_S3_MEM_B
- =PPVDDQ_S3_MEM_B
- =PPDDRVTT_S0_MEM_B
- =PP3V3_S0_MEM_B_SPD (2.5 - 3.3V)

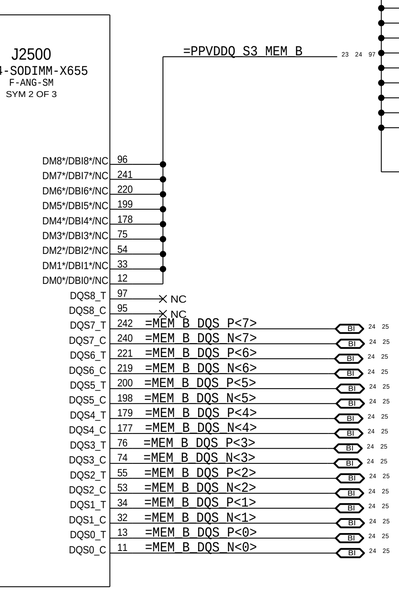
Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

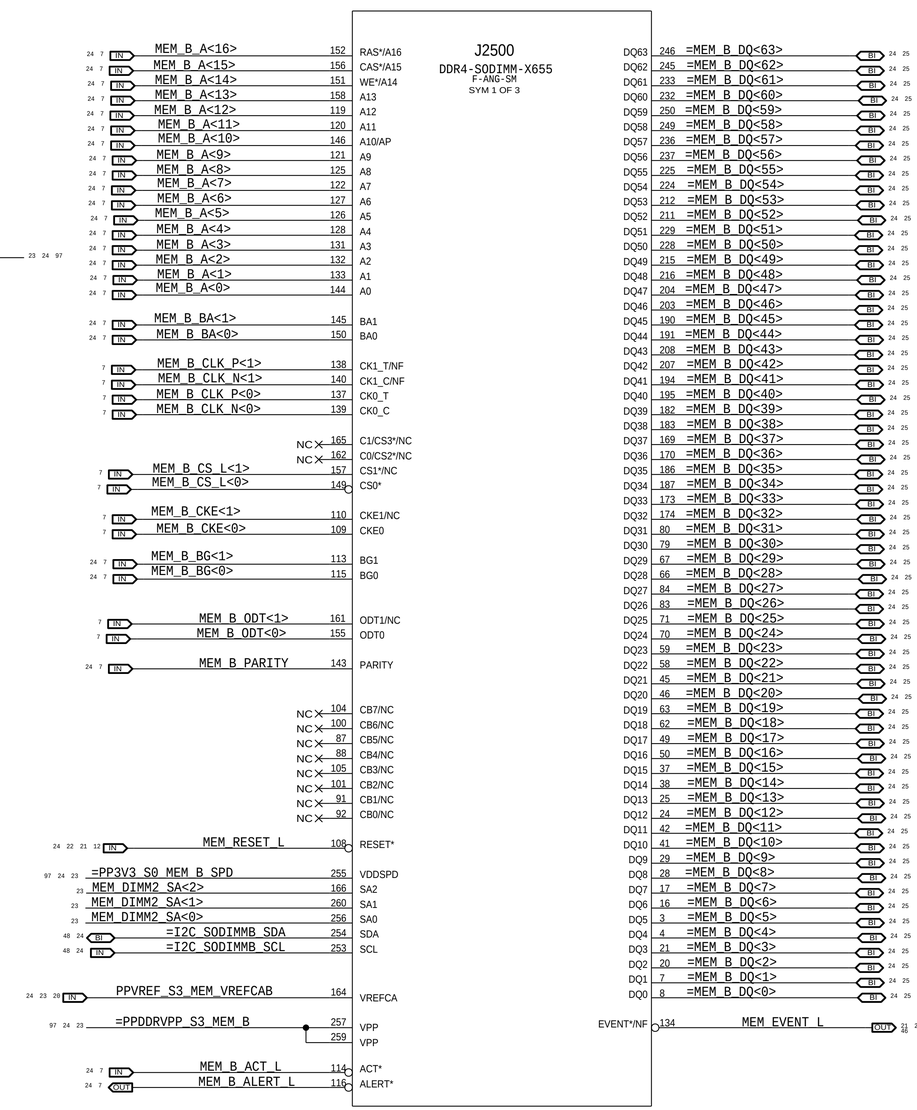
P/N: 516S00204







SKL/KBL DOES NOT SUPPORT DM (DATAMASK)
SIGNAL IS ACTIVE LOW FOR DDR4
RECOMMENDED TO PULL TO VDDQ TO DISABLE FUNCITON



BOM_COST_GROUP=DRAM

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SYNC_MASTER=DORESSLER SYNC_DATE=02/03/2016

PAGE TITLE
DRAM: SO-DIMM CONNECTOR B SLOT0

Apple Inc.

DRAWING NUMBER 051-01506 SIZE D
REVISION 5.19.0
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Page Notes

Power aliases required by this page:
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- =PPVDDQ_S3_MEM_B
- =PPDDRVTT_S0_MEM_B
- =PP3V3_S0_MEM_B_SPD (2.5 - 3.3V)

Signal aliases required by this page:
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- =I2C_SODIMMA_SDA

BOM options provided by this page:
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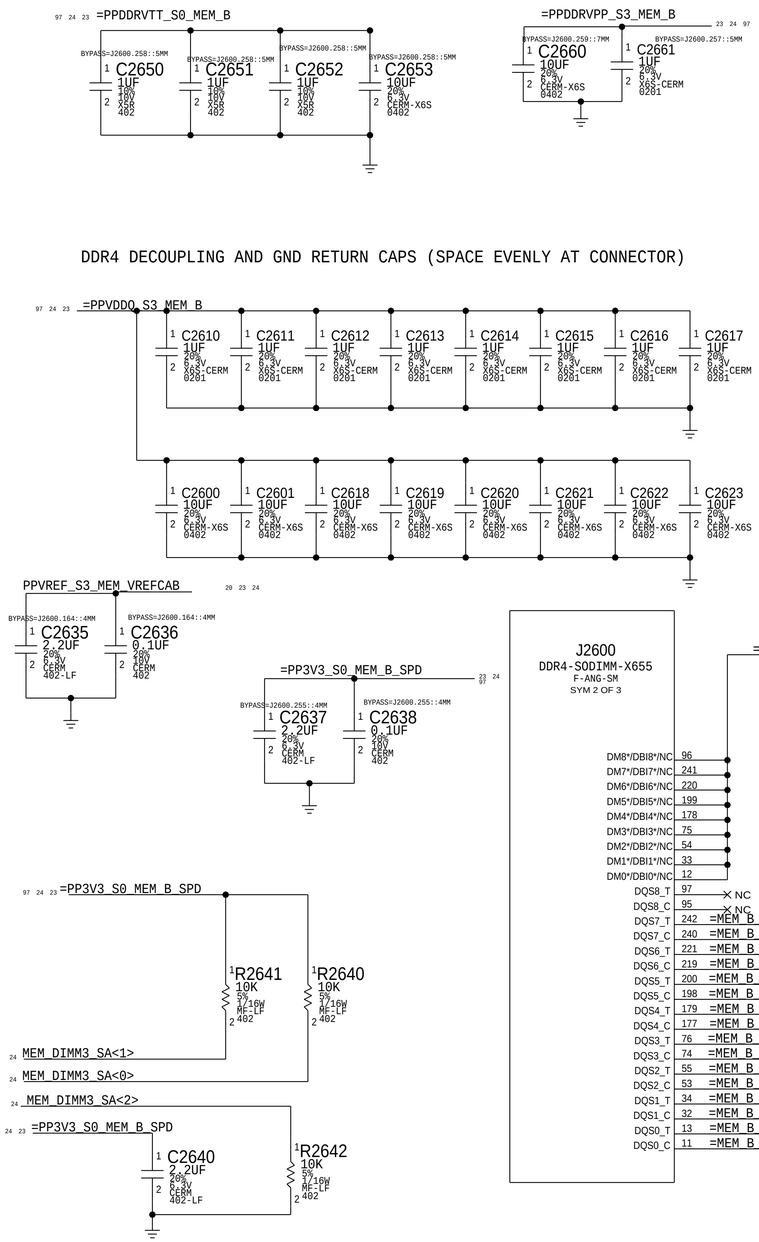
P/N: 516S00204



SKL/KBL DOES NOT SUPPORT DM (DATAMASK)
SIGNAL IS ACTIVE LOW FOR DDR4
RECOMMENDED TO PULL TO VDDQ TO DISABLE FUNCITON

BOM_COST_GROUP=DRAM

SYNC_MASTER=DDRESSLER SYNC_DATE=02/03/2016

PAGE TITLE
DRAM: SO-DIMM CONNECTOR B SLOT1

Apple Inc.

DRAWING NUMBER 051-01506 SIZE D
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THERE ARE DQ PIN SWAPS WITHIN A BYTE

MEM_A_DQS_N<0>	MAKE_BASE=TRUE	=MEM_A_DQS_N<0>	21 22	MEM_B_DQS_N<0>	MAKE_BASE=TRUE	=MEM_B_DQS_N<0>	23 24
MEM_A_DQS_P<0>	MAKE_BASE=TRUE	=MEM_A_DQS_P<0>	21 22	MEM_B_DQS_P<0>	MAKE_BASE=TRUE	=MEM_B_DQS_P<0>	23 24
MEM_A_DQ<7>	MAKE_BASE=TRUE	=MEM_A_DQ<7>	21 22	MEM_B_DQ<7>	MAKE_BASE=TRUE	=MEM_B_DQ<2>	23 24
MEM_A_DQ<6>	MAKE_BASE=TRUE	=MEM_A_DQ<6>	21 22	MEM_B_DQ<6>	MAKE_BASE=TRUE	=MEM_B_DQ<3>	23 24
MEM_A_DQ<5>	MAKE_BASE=TRUE	=MEM_A_DQ<0>	21 22	MEM_B_DQ<5>	MAKE_BASE=TRUE	=MEM_B_DQ<0>	23 24
MEM_A_DQ<4>	MAKE_BASE=TRUE	=MEM_A_DQ<1>	21 22	MEM_B_DQ<4>	MAKE_BASE=TRUE	=MEM_B_DQ<1>	23 24
MEM_A_DQ<3>	MAKE_BASE=TRUE	=MEM_A_DQ<2>	21 22	MEM_B_DQ<3>	MAKE_BASE=TRUE	=MEM_B_DQ<7>	23 24
MEM_A_DQ<2>	MAKE_BASE=TRUE	=MEM_A_DQ<3>	21 22	MEM_B_DQ<2>	MAKE_BASE=TRUE	=MEM_B_DQ<6>	23 24
MEM_A_DQ<1>	MAKE_BASE=TRUE	=MEM_A_DQ<4>	21 22	MEM_B_DQ<1>	MAKE_BASE=TRUE	=MEM_B_DQ<5>	23 24
MEM_A_DQ<0>	MAKE_BASE=TRUE	=MEM_A_DQ<5>	21 22	MEM_B_DQ<0>	MAKE_BASE=TRUE	=MEM_B_DQ<4>	23 24
MEM_A_DQS_N<1>	MAKE_BASE=TRUE	=MEM_A_DQS_N<1>	21 22	MEM_B_DQS_N<1>	MAKE_BASE=TRUE	=MEM_B_DQS_N<1>	23 24
MEM_A_DQS_P<1>	MAKE_BASE=TRUE	=MEM_A_DQS_P<1>	21 22	MEM_B_DQS_P<1>	MAKE_BASE=TRUE	=MEM_B_DQS_P<1>	23 24
MEM_A_DQ<15>	MAKE_BASE=TRUE	=MEM_A_DQ<14>	21 22	MEM_B_DQ<15>	MAKE_BASE=TRUE	=MEM_B_DQ<11>	23 24
MEM_A_DQ<14>	MAKE_BASE=TRUE	=MEM_A_DQ<15>	21 22	MEM_B_DQ<14>	MAKE_BASE=TRUE	=MEM_B_DQ<10>	23 24
MEM_A_DQ<13>	MAKE_BASE=TRUE	=MEM_A_DQ<13>	21 22	MEM_B_DQ<13>	MAKE_BASE=TRUE	=MEM_B_DQ<8>	23 24
MEM_A_DQ<12>	MAKE_BASE=TRUE	=MEM_A_DQ<9>	21 22	MEM_B_DQ<12>	MAKE_BASE=TRUE	=MEM_B_DQ<13>	23 24
MEM_A_DQ<11>	MAKE_BASE=TRUE	=MEM_A_DQ<10>	21 22	MEM_B_DQ<11>	MAKE_BASE=TRUE	=MEM_B_DQ<14>	23 24
MEM_A_DQ<10>	MAKE_BASE=TRUE	=MEM_A_DQ<11>	21 22	MEM_B_DQ<10>	MAKE_BASE=TRUE	=MEM_B_DQ<15>	23 24
MEM_A_DQ<9>	MAKE_BASE=TRUE	=MEM_A_DQ<12>	21 22	MEM_B_DQ<9>	MAKE_BASE=TRUE	=MEM_B_DQ<9>	23 24
MEM_A_DQ<8>	MAKE_BASE=TRUE	=MEM_A_DQ<8>	21 22	MEM_B_DQ<8>	MAKE_BASE=TRUE	=MEM_B_DQ<12>	23 24
MEM_A_DQS_N<2>	MAKE_BASE=TRUE	=MEM_A_DQS_N<2>	21 22	MEM_B_DQS_N<2>	MAKE_BASE=TRUE	=MEM_B_DQS_N<2>	23 24
MEM_A_DQS_P<2>	MAKE_BASE=TRUE	=MEM_A_DQS_P<2>	21 22	MEM_B_DQS_P<2>	MAKE_BASE=TRUE	=MEM_B_DQS_P<2>	23 24
MEM_A_DQ<23>	MAKE_BASE=TRUE	=MEM_A_DQ<22>	21 22	MEM_B_DQ<23>	MAKE_BASE=TRUE	=MEM_B_DQ<18>	23 24
MEM_A_DQ<22>	MAKE_BASE=TRUE	=MEM_A_DQ<23>	21 22	MEM_B_DQ<22>	MAKE_BASE=TRUE	=MEM_B_DQ<19>	23 24
MEM_A_DQ<21>	MAKE_BASE=TRUE	=MEM_A_DQ<20>	21 22	MEM_B_DQ<21>	MAKE_BASE=TRUE	=MEM_B_DQ<16>	23 24
MEM_A_DQ<20>	MAKE_BASE=TRUE	=MEM_A_DQ<16>	21 22	MEM_B_DQ<20>	MAKE_BASE=TRUE	=MEM_B_DQ<20>	23 24
MEM_A_DQ<19>	MAKE_BASE=TRUE	=MEM_A_DQ<19>	21 22	MEM_B_DQ<19>	MAKE_BASE=TRUE	=MEM_B_DQ<23>	23 24
MEM_A_DQ<18>	MAKE_BASE=TRUE	=MEM_A_DQ<18>	21 22	MEM_B_DQ<18>	MAKE_BASE=TRUE	=MEM_B_DQ<22>	23 24
MEM_A_DQ<17>	MAKE_BASE=TRUE	=MEM_A_DQ<17>	21 22	MEM_B_DQ<17>	MAKE_BASE=TRUE	=MEM_B_DQ<21>	23 24
MEM_A_DQ<16>	MAKE_BASE=TRUE	=MEM_A_DQ<21>	21 22	MEM_B_DQ<16>	MAKE_BASE=TRUE	=MEM_B_DQ<17>	23 24
MEM_A_DQS_N<3>	MAKE_BASE=TRUE	=MEM_A_DQS_N<3>	21 22	MEM_B_DQS_N<3>	MAKE_BASE=TRUE	=MEM_B_DQS_N<3>	23 24
MEM_A_DQS_P<3>	MAKE_BASE=TRUE	=MEM_A_DQS_P<3>	21 22	MEM_B_DQS_P<3>	MAKE_BASE=TRUE	=MEM_B_DQS_P<3>	23 24
MEM_A_DQ<31>	MAKE_BASE=TRUE	=MEM_A_DQ<27>	21 22	MEM_B_DQ<31>	MAKE_BASE=TRUE	=MEM_B_DQ<26>	23 24
MEM_A_DQ<30>	MAKE_BASE=TRUE	=MEM_A_DQ<30>	21 22	MEM_B_DQ<30>	MAKE_BASE=TRUE	=MEM_B_DQ<27>	23 24
MEM_A_DQ<29>	MAKE_BASE=TRUE	=MEM_A_DQ<25>	21 22	MEM_B_DQ<29>	MAKE_BASE=TRUE	=MEM_B_DQ<24>	23 24
MEM_A_DQ<28>	MAKE_BASE=TRUE	=MEM_A_DQ<29>	21 22	MEM_B_DQ<28>	MAKE_BASE=TRUE	=MEM_B_DQ<25>	23 24
MEM_A_DQ<27>	MAKE_BASE=TRUE	=MEM_A_DQ<31>	21 22	MEM_B_DQ<27>	MAKE_BASE=TRUE	=MEM_B_DQ<30>	23 24
MEM_A_DQ<26>	MAKE_BASE=TRUE	=MEM_A_DQ<26>	21 22	MEM_B_DQ<26>	MAKE_BASE=TRUE	=MEM_B_DQ<31>	23 24
MEM_A_DQ<25>	MAKE_BASE=TRUE	=MEM_A_DQ<28>	21 22	MEM_B_DQ<25>	MAKE_BASE=TRUE	=MEM_B_DQ<29>	23 24
MEM_A_DQ<24>	MAKE_BASE=TRUE	=MEM_A_DQ<24>	21 22	MEM_B_DQ<24>	MAKE_BASE=TRUE	=MEM_B_DQ<28>	23 24
MEM_A_DQS_N<4>	MAKE_BASE=TRUE	=MEM_A_DQS_N<4>	21 22	MEM_B_DQS_N<4>	MAKE_BASE=TRUE	=MEM_B_DQS_N<4>	23 24
MEM_A_DQS_P<4>	MAKE_BASE=TRUE	=MEM_A_DQS_P<4>	21 22	MEM_B_DQS_P<4>	MAKE_BASE=TRUE	=MEM_B_DQS_P<4>	23 24
MEM_A_DQ<39>	MAKE_BASE=TRUE	=MEM_A_DQ<39>	21 22	MEM_B_DQ<39>	MAKE_BASE=TRUE	=MEM_B_DQ<35>	23 24
MEM_A_DQ<38>	MAKE_BASE=TRUE	=MEM_A_DQ<38>	21 22	MEM_B_DQ<38>	MAKE_BASE=TRUE	=MEM_B_DQ<39>	23 24
MEM_A_DQ<37>	MAKE_BASE=TRUE	=MEM_A_DQ<36>	21 22	MEM_B_DQ<37>	MAKE_BASE=TRUE	=MEM_B_DQ<32>	23 24
MEM_A_DQ<36>	MAKE_BASE=TRUE	=MEM_A_DQ<37>	21 22	MEM_B_DQ<36>	MAKE_BASE=TRUE	=MEM_B_DQ<37>	23 24
MEM_A_DQ<35>	MAKE_BASE=TRUE	=MEM_A_DQ<34>	21 22	MEM_B_DQ<35>	MAKE_BASE=TRUE	=MEM_B_DQ<34>	23 24
MEM_A_DQ<34>	MAKE_BASE=TRUE	=MEM_A_DQ<35>	21 22	MEM_B_DQ<34>	MAKE_BASE=TRUE	=MEM_B_DQ<38>	23 24
MEM_A_DQ<33>	MAKE_BASE=TRUE	=MEM_A_DQ<33>	21 22	MEM_B_DQ<33>	MAKE_BASE=TRUE	=MEM_B_DQ<33>	23 24
MEM_A_DQ<32>	MAKE_BASE=TRUE	=MEM_A_DQ<32>	21 22	MEM_B_DQ<32>	MAKE_BASE=TRUE	=MEM_B_DQ<36>	23 24
MEM_A_DQS_N<5>	MAKE_BASE=TRUE	=MEM_A_DQS_N<5>	21 22	MEM_B_DQS_N<5>	MAKE_BASE=TRUE	=MEM_B_DQS_N<5>	23 24
MEM_A_DQS_P<5>	MAKE_BASE=TRUE	=MEM_A_DQS_P<5>	21 22	MEM_B_DQS_P<5>	MAKE_BASE=TRUE	=MEM_B_DQS_P<5>	23 24
MEM_A_DQ<47>	MAKE_BASE=TRUE	=MEM_A_DQ<43>	21 22	MEM_B_DQ<47>	MAKE_BASE=TRUE	=MEM_B_DQ<43>	23 24
MEM_A_DQ<46>	MAKE_BASE=TRUE	=MEM_A_DQ<46>	21 22	MEM_B_DQ<46>	MAKE_BASE=TRUE	=MEM_B_DQ<42>	23 24
MEM_A_DQ<45>	MAKE_BASE=TRUE	=MEM_A_DQ<44>	21 22	MEM_B_DQ<45>	MAKE_BASE=TRUE	=MEM_B_DQ<44>	23 24
MEM_A_DQ<44>	MAKE_BASE=TRUE	=MEM_A_DQ<40>	21 22	MEM_B_DQ<44>	MAKE_BASE=TRUE	=MEM_B_DQ<40>	23 24
MEM_A_DQ<43>	MAKE_BASE=TRUE	=MEM_A_DQ<47>	21 22	MEM_B_DQ<43>	MAKE_BASE=TRUE	=MEM_B_DQ<46>	23 24
MEM_A_DQ<42>	MAKE_BASE=TRUE	=MEM_A_DQ<42>	21 22	MEM_B_DQ<42>	MAKE_BASE=TRUE	=MEM_B_DQ<47>	23 24
MEM_A_DQ<41>	MAKE_BASE=TRUE	=MEM_A_DQ<45>	21 22	MEM_B_DQ<41>	MAKE_BASE=TRUE	=MEM_B_DQ<41>	23 24
MEM_A_DQ<40>	MAKE_BASE=TRUE	=MEM_A_DQ<41>	21 22	MEM_B_DQ<40>	MAKE_BASE=TRUE	=MEM_B_DQ<45>	23 24
MEM_A_DQS_N<6>	MAKE_BASE=TRUE	=MEM_A_DQS_N<6>	21 22	MEM_B_DQS_N<6>	MAKE_BASE=TRUE	=MEM_B_DQS_N<6>	23 24
MEM_A_DQS_P<6>	MAKE_BASE=TRUE	=MEM_A_DQS_P<6>	21 22	MEM_B_DQS_P<6>	MAKE_BASE=TRUE	=MEM_B_DQS_P<6>	23 24
MEM_A_DQ<55>	MAKE_BASE=TRUE	=MEM_A_DQ<54>	21 22	MEM_B_DQ<55>	MAKE_BASE=TRUE	=MEM_B_DQ<50>	23 24
MEM_A_DQ<54>	MAKE_BASE=TRUE	=MEM_A_DQ<49>	21 22	MEM_B_DQ<54>	MAKE_BASE=TRUE	=MEM_B_DQ<54>	23 24
MEM_A_DQ<53>	MAKE_BASE=TRUE	=MEM_A_DQ<55>	21 22	MEM_B_DQ<53>	MAKE_BASE=TRUE	=MEM_B_DQ<48>	23 24
MEM_A_DQ<52>	MAKE_BASE=TRUE	=MEM_A_DQ<53>	21 22	MEM_B_DQ<52>	MAKE_BASE=TRUE	=MEM_B_DQ<49>	23 24
MEM_A_DQ<51>	MAKE_BASE=TRUE	=MEM_A_DQ<51>	21 22	MEM_B_DQ<51>	MAKE_BASE=TRUE	=MEM_B_DQ<51>	23 24
MEM_A_DQ<50>	MAKE_BASE=TRUE	=MEM_A_DQ<52>	21 22	MEM_B_DQ<50>	MAKE_BASE=TRUE	=MEM_B_DQ<55>	23 24
MEM_A_DQ<49>	MAKE_BASE=TRUE	=MEM_A_DQ<50>	21 22	MEM_B_DQ<49>	MAKE_BASE=TRUE	=MEM_B_DQ<52>	23 24
MEM_A_DQ<48>	MAKE_BASE=TRUE	=MEM_A_DQ<48>	21 22	MEM_B_DQ<48>	MAKE_BASE=TRUE	=MEM_B_DQ<53>	23 24
MEM_A_DQS_N<7>	MAKE_BASE=TRUE	=MEM_A_DQS_N<7>	21 22	MEM_B_DQS_N<7>	MAKE_BASE=TRUE	=MEM_B_DQS_N<7>	23 24
MEM_A_DQS_P<7>	MAKE_BASE=TRUE	=MEM_A_DQS_P<7>	21 22	MEM_B_DQS_P<7>	MAKE_BASE=TRUE	=MEM_B_DQS_P<7>	23 24
MEM_A_DQ<63>	MAKE_BASE=TRUE	=MEM_A_DQ<57>	21 22	MEM_B_DQ<63>	MAKE_BASE=TRUE	=MEM_B_DQ<59>	23 24
MEM_A_DQ<62>	MAKE_BASE=TRUE	=MEM_A_DQ<59>	21 22	MEM_B_DQ<62>	MAKE_BASE=TRUE	=MEM_B_DQ<63>	23 24
MEM_A_DQ<61>	MAKE_BASE=TRUE	=MEM_A_DQ<56>	21 22	MEM_B_DQ<61>	MAKE_BASE=TRUE	=MEM_B_DQ<56>	23 24
MEM_A_DQ<60>	MAKE_BASE=TRUE	=MEM_A_DQ<62>	21 22	MEM_B_DQ<60>	MAKE_BASE=TRUE	=MEM_B_DQ<60>	23 24
MEM_A_DQ<59>	MAKE_BASE=TRUE	=MEM_A_DQ<58>	21 22	MEM_B_DQ<59>	MAKE_BASE=TRUE	=MEM_B_DQ<62>	23 24
MEM_A_DQ<58>	MAKE_BASE=TRUE	=MEM_A_DQ<60>	21 22	MEM_B_DQ<58>	MAKE_BASE=TRUE	=MEM_B_DQ<58>	23 24
MEM_A_DQ<57>	MAKE_BASE=TRUE	=MEM_A_DQ<63>	21 22	MEM_B_DQ<57>	MAKE_BASE=TRUE	=MEM_B_DQ<61>	23 24
MEM_A_DQ<56>	MAKE_BASE=TRUE	=MEM_A_DQ<61>	21 22	MEM_B_DQ<56>	MAKE_BASE=TRUE	=MEM_B_DQ<57>	23 24

https://vinafix.com

BOM_COST_GROUP=DRAM

SYNC_MASTER=DDRESSLER SYNC_DATE=02/03/2016

PAGE TITLE
DRAM: ALIASES AND BITSWAPS

Apple Inc.

DRAWING NUMBER 051-01506 SIZE D

REVISION 5.19.0

BRANCH

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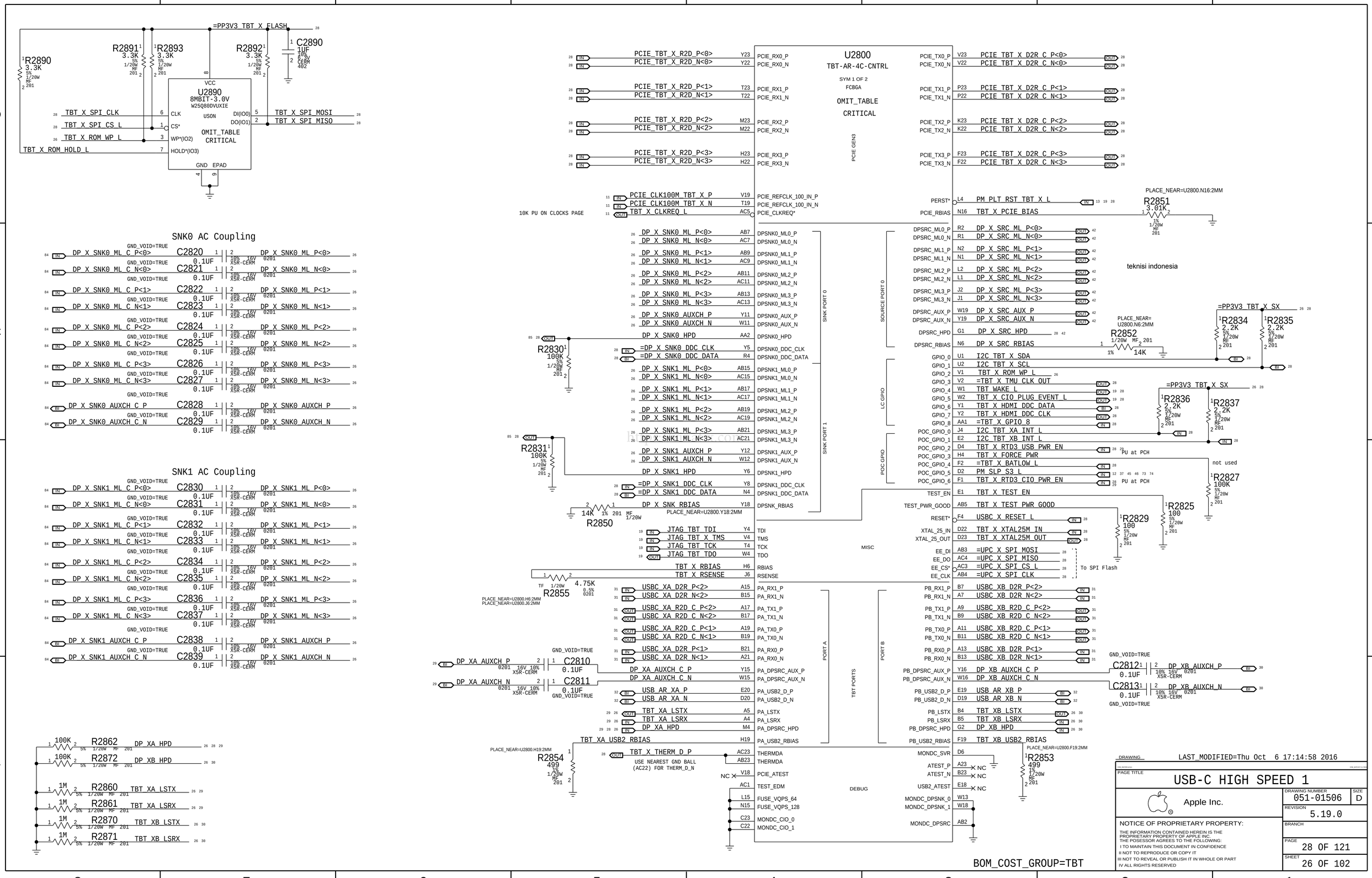
=PP3V3_TBT_X_FLASH
R2890 3.3K 5% 1/20W MF 201
R2891 3.3K 5% 1/20W MF 201
R2893 3.3K 5% 1/20W MF 201
R2892 3.3K 5% 1/20W MF 201
C2890 1UF 10% 6.3V CERM 402
U2890 8MBIT-3.0V W25Q80DVUXIE USON
OMIT_TABLE CRITICAL
TBT_X_SPI_CLK
TBT_X_SPI_CS_L
TBT_X_ROM_WP_L
TBT_X_ROM_HOLD_L
TBT_X_SPI_MOSI
TBT_X_SPI_MISO
SNK0 AC Coupling
SNK1 AC Coupling
U2800 TBT-AR-4C-CNTRL
SYM 1 OF 2 FCBGA
OMIT_TABLE CRITICAL
PCIE GEN3
10K PU ON CLOCKS PAGE
PLACE_NEAR=U2800.N16:2MM
R2851 3.01K 1% 1/20W MF 201
teknisi indonesia
PLACE_NEAR= U2800.N6:2MM
R2852 14K 1% 1/20W MF 201
=PP3V3_TBT_X_SX
R2834 2.2K 5% 1/20W MF 201
R2835 2.2K 5% 1/20W MF 201
R2836 2.2K 5% 1/20W MF 201
R2837 2.2K 5% 1/20W MF 201
R2827 100K 5% 1/20W MF 201
not used
PU at PCH
R2829 100 5% 1/20W MF 201
R2825 100 5% 1/20W MF 201
To SPI Flash
R2830 100K 5% 1/20W MF 201
R2831 100K 5% 1/20W MF 201
R2850 14K 1% 201 MF 1/20W
PLACE_NEAR=U2800.Y18:2MM
R2855 4.75K 0.5% 0201
PLACE_NEAR=U2800.H6:2MM
PLACE_NEAR=U2800.J6:2MM
R2854 499 1% 1/20W MF 201
USE NEAREST GND BALL (AC22) FOR THERM_D_N
R2853 499 1% 1/20W MF 201
PLACE_NEAR=U2800.F19:2MM
R2862 100K 5% 1/20W MF 201 DP_XA_HPD
R2872 100K 5% 1/20W MF 201 DP_XB_HPD
R2860 1M 5% 1/20W MF 201 TBT_XA_LSTX
R2861 1M 5% 1/20W MF 201 TBT_XB_LSTX
R2870 1M 5% 1/20W MF 201 TBT_XB_LSTX
R2871 1M 5% 1/20W MF 201 TBT_XB_LSRX
BOM_COST_GROUP=TBT
DRAWING LAST_MODIFIED=Thu Oct 6 17:14:58 2016
PAGE TITLE USB-C HIGH SPEED 1
Apple Inc.
DRAWING NUMBER 051-01506
SIZE D
REVISION 5.19.0
BRANCH
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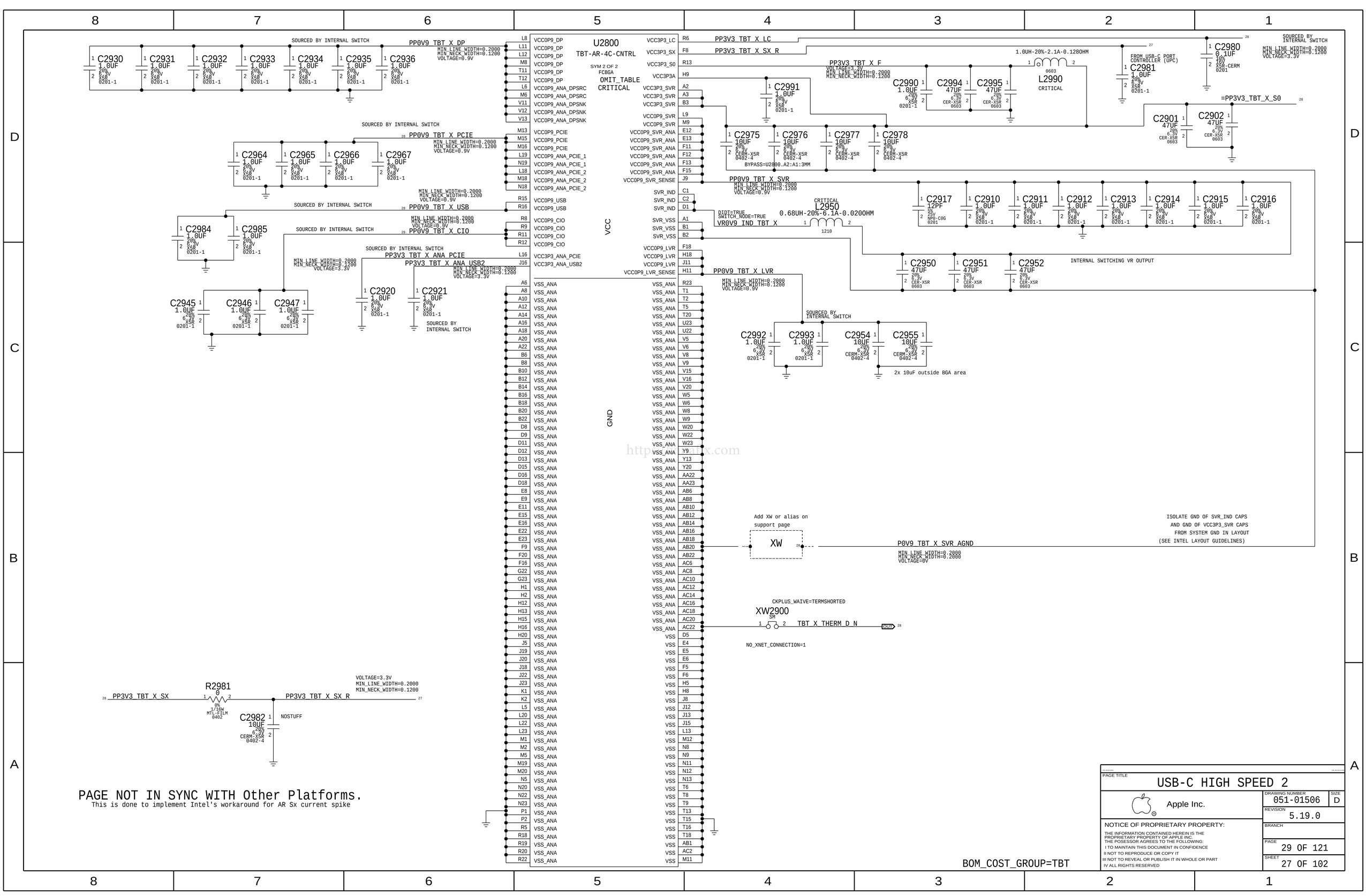
U2800
TBT-AR-4C-CNTRL
SYM 2 OF 2
FCBGA
OMIT_TABLE
CRITICAL
VCC
GND
SOURCED BY INTERNAL SWITCH
PP0V9_TBT_X_DP
PP0V9_TBT_X_PCIE
PP0V9_TBT_X_USB
PP0V9_TBT_X_CIO
PP3V3_TBT_X_ANA_PCIE
PP3V3_TBT_X_ANA_USB2
PP3V3_TBT_X_LC
PP3V3_TBT_X_SX_R
PP3V3_TBT_X_F
PP3V3_TBT_X_S0
PP0V9_TBT_X_SVR
PP0V9_TBT_X_LVR
VR0V9_IND_TBT_X
L2950
0.68UH-20%-6.1A-0.020OHM
L2990
CRITICAL
1.0UH-20%-2.1A-0.1280HM
FROM USB-C PORT CONTROLLER (UPC)
INTERNAL SWITCHING VR OUTPUT
2x 10uF outside BGA area
Add XW or alias on support page
XW
P0V9_TBT_X_SVR_AGND
ISOLATE GND OF SVR_IND CAPS AND GND OF VCC3P3_SVR CAPS FROM SYSTEM GND IN LAYOUT (SEE INTEL LAYOUT GUIDELINES)
XW2900
TBT_X_THERM_D_N
NO_XNET_CONNECTION=1
R2981
PP3V3_TBT_X_SX
PP3V3_TBT_X_SX_R
C2982
NOSTUFF
PAGE NOT IN SYNC WITH Other Platforms.
This is done to implement Intel's workaround for AR Sx current spike
BOM_COST_GROUP=TBT
PAGE TITLE
USB-C HIGH SPEED 2
Apple Inc.
DRAWING NUMBER 051-01506
SIZE D
REVISION 5.19.0
BRANCH
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Ridge PUs

=TBT_X_BATLOW_L — MAKE_BASE=TRUE PM_BATLOW_L — R3075 100K 1/20W 201 5% MF — PP3V3_TBT_X_SX

TBT_X_HDMI_DDC_CLK — R3074 100K 1/20W 201 MF 5% — PP3V3_TBT_X_LC

USBC 5V EN PD

UPC_XA_5V_EN — R3032 100K 1/20W MF 201 5% 2

UPC_XB_5V_EN — R3012 100K 1/20W MF 201 5% 2

ACE Debug Support

TP_UPC_XA_DBG_UART_TX — NOSTUFF R3089 NOSTUFF NONE NONE NONE 402 — TP_UPC_XA_DBG_UART_RX

TP_UPC_XB_DBG_UART_TX — NOSTUFF R3088 NOSTUFF NONE NONE NONE 402 — TP_UPC_XB_DBG_UART_RX

Ridge PDs

=DP_X_SNK0_DDC_CLK — MAKE_BASE=TRUE DP_X_SNK0_DDC_CLK — R3067 100K 1/20W MF 201 5%

=DP_X_SNK0_DDC_DATA — MAKE_BASE=TRUE DP_X_SNK0_DDC_DATA — R3068 100K 1/20W MF 201 5%

=DP_X_SNK1_DDC_CLK — MAKE_BASE=TRUE DP_X_SNK1_DDC_CLK — R3069 100K 1/20W MF 201 5%

=DP_X_SNK1_DDC_DATA — MAKE_BASE=TRUE DP_X_SNK1_DDC_DATA — R3070 100K 1/20W MF 201 5%

=TBT_X_GPIO_8 — MAKE_BASE=TRUE PD_TBT_X_GPIO_8 — R3071 100K 1/20W MF 201 5%

=TBT_X_TMU_CLK_OUT — MAKE_BASE=TRUE PD_TBT_X_TMU_CLK_OUT — R3072 100K 1/20W MF 201 5%

DP_X_SRC_HPD — R3073 100K 1/20W MF 201 5%

TBT_X_HDMI_DDC_DATA — R3076 100K 1/20W MF 201 5%

SMC RESET Connection

UPC_XA_HPD_RX — R3033 100K 1/20W MF 201 5% — R3024 0 1/20W MF 0201 5% NOSTUFF

UPC_XB_HPD_RX — R3034 0 1/20W MF 0201 5% NOSTUFF — SMC_RESET_L

R3025 100K 1/20W MF 201 5%

GND ALIASES

USBC_XB_RPD_G2
USBC_XB_RPD_G1
USBC_XA_RPD_G2
USBC_XA_RPD_G1
UPC_XB_SPI_CLK
UPC_XB_SPI_MOSI
UPC_XB_SPI_MISO
UPC_XB_SPI_CS_L
UPC_XA_RESET
UPC_XB_RESET
TBT_X_THERM_D_P
TBT_X_THERM_D_N

MAKE_BASE=TRUE

I2C SERIES R'S

PLACE_NEAR=U5000:5mm

=I2C_UPC_XA_SDA2 — R3041 33 1/20W MF 201 5% — =I2C_UPC_XA_SDA2_R

=I2C_UPC_XB_SDA2 — MAKE_BASE=TRUE — =I2C_UPC_XB_SDA2_R

I2C_UPC_X_SDA2

PLACE_NEAR=U5000:5mm

=I2C_UPC_XA_SCL2 — R3042 33 1/20W MF 201 5% — =I2C_UPC_XA_SCL2_R

=I2C_UPC_XB_SCL2 — MAKE_BASE=TRUE — =I2C_UPC_XB_SCL2_R

I2C_UPC_X_SCL2

RIDGE 0.9V SVR XW

XW3000 SM

P0V9_TBT_X_SVR_AGND

NO_XNET_CONNECTION=1

POWER ALIASES

=PP5V_USBC_XA
=PP5V_USBC_XB
=PP5V_S4_USBC

=PP3V3_TBT_X_S0 — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V — PP3V3_TBT_X_S0 — MAKE_BASE=TRUE — XW3001 SM — =PP3V3_TBT_X_S0_R

=PPHV_TBT_XA
=PPHV_TBT_XB
=PPHV_SW_TBT_X

=PP3V3_TBT_X_SX
=PP3V3_UPC_XA_SX
=PP3V3_UPC_XB_SX — MAKE_BASE=TRUE PP3V3_TBT_X_SX — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=3.3V

=PP3V3R1V8_UPC_XB
=PP3V3_UPC_XB_LDO — MAKE_BASE=TRUE PP3V3_UPC_XB_LDO — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V

=PP3V3_TBT_X_FLASH
=PP3V3R1V8_UPC_XA
=PP3V3_UPC_XA_LDO — MAKE_BASE=TRUE PP3V3_UPC_XA_LDO — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V

TBT to ACE

TBT
Alpine Ridge U2800
(MASTER)

Pri ACE
U3100
(Write: 0x70 Read: 0x71)

PLACE_NEAR=U2800:10MM

I2C_TBT_X_SCL — R3047 33 1/20W MF 201 5% — I2C_TBT_SCL_R — MAKE_BASE=TRUE — =I2C_UPC_XA_SCL1

I2C_TBT_X_SDA — R3048 33 1/20W MF 201 5% — I2C_TBT_SDA_R — MAKE_BASE=TRUE — =I2C_UPC_XA_SDA1

PLACE_NEAR=U2800:10MM

MAKE_BASE=TRUE — I2C_TBT_XA_INT_L — =I2C_UPC_XA_INT1_L

MAKE_BASE=TRUE — I2C_TBT_XB_INT_L

Sec ACE
U3200
(Write: 0x7E Read: 0x7F)

=I2C_UPC_XB_SCL1
=I2C_UPC_XB_SDA1
=I2C_UPC_XB_INT1_L

RIDGE DEBUG CONN

Place on bottom

BOM OPTION Removed
No Stuff at PVT

J3099 505070-1220 M-ST-SM — DEVELOPMENT

TBT_X_CIO_PLUG_EVENT_L	1	2	PM_PLT_RST_TBT_X_L
DP_X_SNK0_HPD	3	4	USBC_X_RESET_L
ARKANOID_P5	5	6	PP3V3_TBT_X_SX
ARKANOID_P7	7	8	PP0V9_TBT_X_PCIE
TBT_POC_RESET	9	10	PP0V9_TBT_X_USB
PP3V3_TBT_X_LC	11	12	PP0V9_TBT_X_CIO

516S00115

ACE DEBUG CONN

Place on bottom

BOM OPTION Removed
No Stuff at PVT

J3000 505070-1220 M-ST-SM — DEVELOPMENT

I2C_TBT_XB_INT_L	1	2	I2C_TBT_XA_INT_L
I2C_UPC_X_SCL2	3	4	I2C_TBT_X_SDA
I2C_UPC_X_SDA2	5	6	I2C_TBT_X_SCL
SMC_USBC_INT_L	7	8	I2C_UPC_XB_DBG_CTL_SDA
TBT_X_SPI_CLK_DBG	9	10	I2C_UPC_XB_DBG_CTL_SCL
UPC_XA_UART_TX	11	12	UPC_XA_UART_RX

SIGNAL ALIASES

TBT_X_RTD3_CIO_PWR_EN — MAKE_BASE=TBT_X_CIO_PWR_EN
UPC_XB_GPIO2

TBT_X_RTD3_USB_PWR_EN — MAKE_BASE=TBT_X_USB_PWR_EN
UPC_XB_GPIO3

=UPC_WAKE_L — MAKE_BASE=TBT_WAKE_L

=UPC_X_SPI_CLK — MAKE_BASE=UPC_X_SPI_CLK
=UPC_X_SPI_CS_L — MAKE_BASE=UPC_X_SPI_CS_L
=UPC_X_SPI_MOSI — MAKE_BASE=UPC_X_SPI_MOSI
=UPC_X_SPI_MISO — MAKE_BASE=UPC_X_SPI_MISO

USBC_X_POC_RESET — MAKE_BASE=TBT_POC_RESET

Ridge PCIE Caps

PCIE_TBT_X_R2D_C_P<0>	C3040	0.22UF	PCIE_TBT_X_R2D_P<0>	GND_VOID=TRUE
PCIE_TBT_X_R2D_C_N<0>	C3041	0.22UF	PCIE_TBT_X_R2D_N<0>	GND_VOID=TRUE
PCIE_TBT_X_R2D_C_P<1>	C3042	0.22UF	PCIE_TBT_X_R2D_P<1>	GND_VOID=TRUE
PCIE_TBT_X_R2D_C_N<1>	C3043	0.22UF	PCIE_TBT_X_R2D_N<1>	GND_VOID=TRUE
PCIE_TBT_X_R2D_C_P<2>	C3044	0.22UF	PCIE_TBT_X_R2D_P<2>	GND_VOID=TRUE
PCIE_TBT_X_R2D_C_N<2>	C3045	0.22UF	PCIE_TBT_X_R2D_N<2>	GND_VOID=TRUE
PCIE_TBT_X_R2D_C_P<3>	C3046	0.22UF	PCIE_TBT_X_R2D_P<3>	GND_VOID=TRUE
PCIE_TBT_X_R2D_C_N<3>	C3047	0.22UF	PCIE_TBT_X_R2D_N<3>	GND_VOID=TRUE
PCIE_TBT_X_D2R_C_P<0>	C3050	0.22UF	PCIE_TBT_X_D2R_P<0>	GND_VOID=TRUE
PCIE_TBT_X_D2R_C_N<0>	C3051	0.22UF	PCIE_TBT_X_D2R_N<0>	GND_VOID=TRUE
PCIE_TBT_X_D2R_C_P<1>	C3052	0.22UF	PCIE_TBT_X_D2R_P<1>	GND_VOID=TRUE
PCIE_TBT_X_D2R_C_N<1>	C3053	0.22UF	PCIE_TBT_X_D2R_N<1>	GND_VOID=TRUE
PCIE_TBT_X_D2R_C_P<2>	C3054	0.22UF	PCIE_TBT_X_D2R_P<2>	GND_VOID=TRUE
PCIE_TBT_X_D2R_C_N<2>	C3055	0.22UF	PCIE_TBT_X_D2R_N<2>	GND_VOID=TRUE
PCIE_TBT_X_D2R_C_P<3>	C3056	0.22UF	PCIE_TBT_X_D2R_P<3>	GND_VOID=TRUE
PCIE_TBT_X_D2R_C_N<3>	C3057	0.22UF	PCIE_TBT_X_D2R_N<3>	GND_VOID=TRUE

AR/ACE SPI BUS SERIES R'S

USBC DEBUG CONN

TBT_X_SPI_CLK	R3094 100	TBT_X_SPI_CLK_DBG		
TBT_X_SPI_CS_L	R3095 15	UPC_XA_SPI_CLK	IN	Ace
TBT_X_SPI_MOSI	R3096 15	UPC_XA_SPI_CS_L	IN	Ace
TBT_X_SPI_MISO	R3097 15	UPC_XA_SPI_MOSI	IN	Ace
ROM	R3098 15	UPC_XA_SPI_MISO	OUT	Ace
	R3090 15	=UPC_X_SPI_CLK	IN	AR
	R3091 15	=UPC_X_SPI_CS_L	IN	AR
	R3092 15	=UPC_X_SPI_MOSI	IN	AR
	R3093 15	=UPC_X_SPI_MISO	OUT	AR

=PP5V_S4_USBC — C3089 220UF-35MOHM 20% 35V POLY-TANT CASE-B2-SM1

ACE XA DEBUG PORTS

SMC SWD	MAKE_BASE=TRUE	SMC_TCK	UPC_XA_DBG1
	MAKE_BASE=TRUE	SMC_TMS	UPC_XA_DBG2
	MAKE_BASE=TRUE	SMC_TX_L	UPC_XA_DBG3
	MAKE_BASE=TRUE	SMC_RX_L	UPC_XA_DBG4

ARKANOID_P5 — R3082 0 MF 0201 5% 1/20W — DP_X_SNK1_HPD
R3083 0 NOSTUFF MF 0201 5% 1/20W — SMC_DEBUGPRT_RX_L

ARKANOID_P7 — R3084 0 MF 0201 5% 1/20W — DP_XA_HPD
R3085 0 NOSTUFF MF 0201 5% 1/20W — SMC_DEBUGPRT_TX_L

ACE XB DEBUG PORTS

R3062 100K 201 MF 1/20W 5% — UPC_XB_DBG1
R3063 100K 201 MF 1/20W 5% — UPC_XB_DBG2

SMC_DEBUGPRT_TX_L — R3080 0 MF 0201 5% 1/20W NOSTUFF — UPC_XB_DBG3

R3015 100K MF 201 5% 1/20W

R3016 100K MF 201 5% 1/20W

SMC MOJO — SMC_DEBUGPRT_RX_L — R3081 0 MF 0201 5% 1/20W NOSTUFF — UPC_XB_DBG4

Place Resistors close to USB-A Mojo Mux resistors.

PPVBUS_USBC_XA_CONN (MAKE_BASE=TRUE)	TP_PPVBUS_USBC_XA	TP3025
PPVBUS_USBC_XB_CONN (MAKE_BASE=TRUE)	TP_PPVBUS_USBC_XB	TP3026
TP_UPC_XA_SWD_DATA		TP3001
TP_UPC_XA_SWD_CLK		TP3002
TP_UPC_XB_SWD_DATA		TP3003
TP_UPC_XB_SWD_CLK		TP3004
=USBC_XB_RESET_L	MAKE_BASE=TRUE TP_USBC_XB_RESET_L	TP3014

USBC_X_RESET_L

=USBC_XA_RESET_L — R3031 0 1/20W MF 201 5% — MAKE_BASE=TRUE USBC_X_RESET_L — C3031 1.0UF 20% 6.3V X5R 0201-1 NOSTUFF

MAKE_BASE=TRUE USBC_X_RESET_L_R — D3000 0201 RB521ES-30 NOSTUFF

25MHz xtal

TBT_X_XTAL25M_OUT — R3007 0 1/20W MF 201 5% — TBT_X_XTAL25M_OUT_R — C3002 20PF 25V C0G 0201 — PLACE_NEAR=Y3000:3.2MM

NOSTUFF R3006 1M 1/20W MF 201 5%

to/from Ridge

CRITICAL Y3000 25MHZ-25PPM-20PF-50OHM 2.00X1.60-SM — PLACE_NEAR=Y3000:3.2MM

C3003 20PF 25V C0G 0201 — PLACE_NEAR=Y3000:1.2MM

TBT_X_XTAL25M_IN

BOM_COST_GROUP=USB-C

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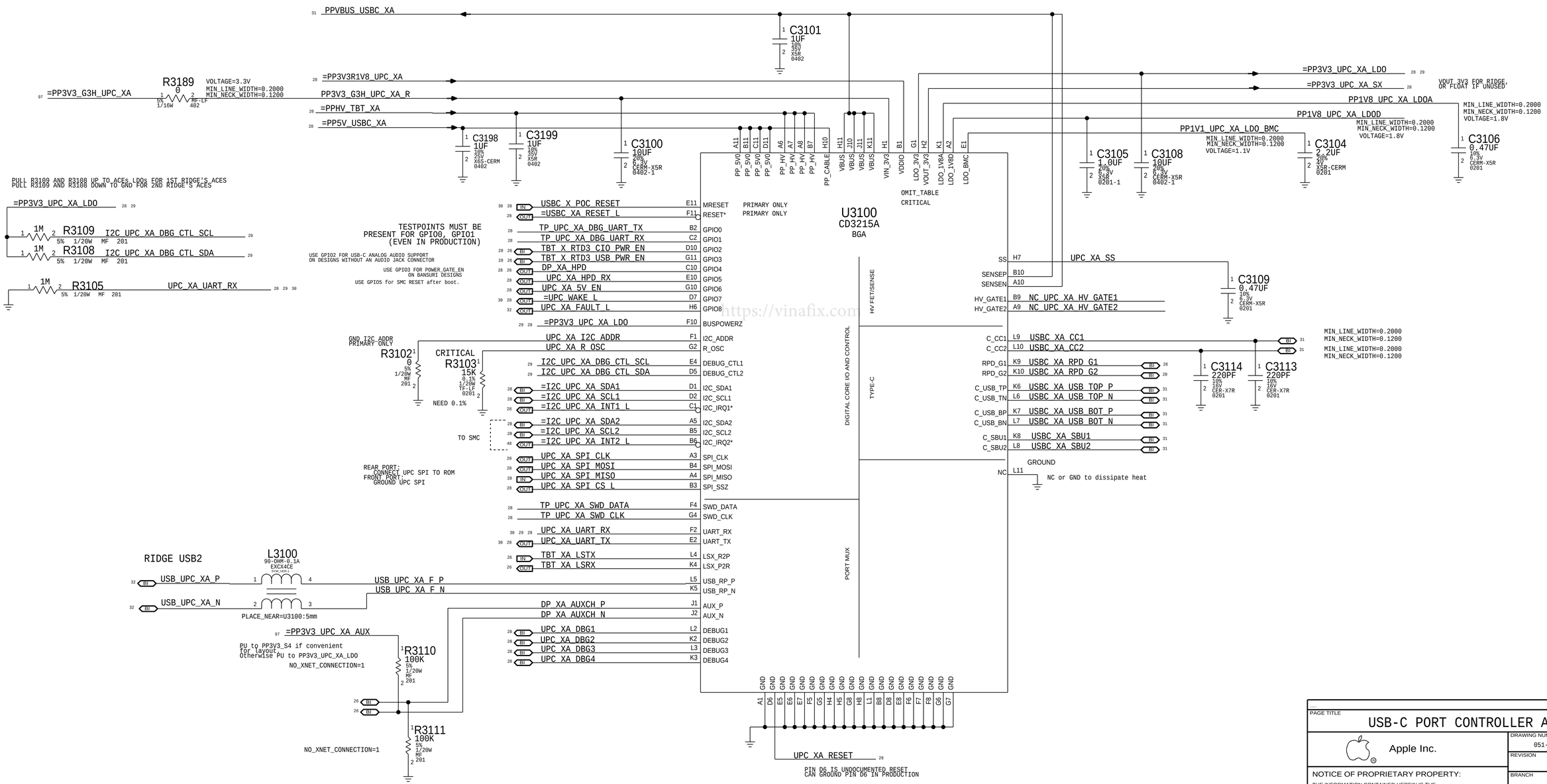
PRIMARY ACE USB-C PORT CONTROLLER (UPC)



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USB-C PORT CONTROLLER A

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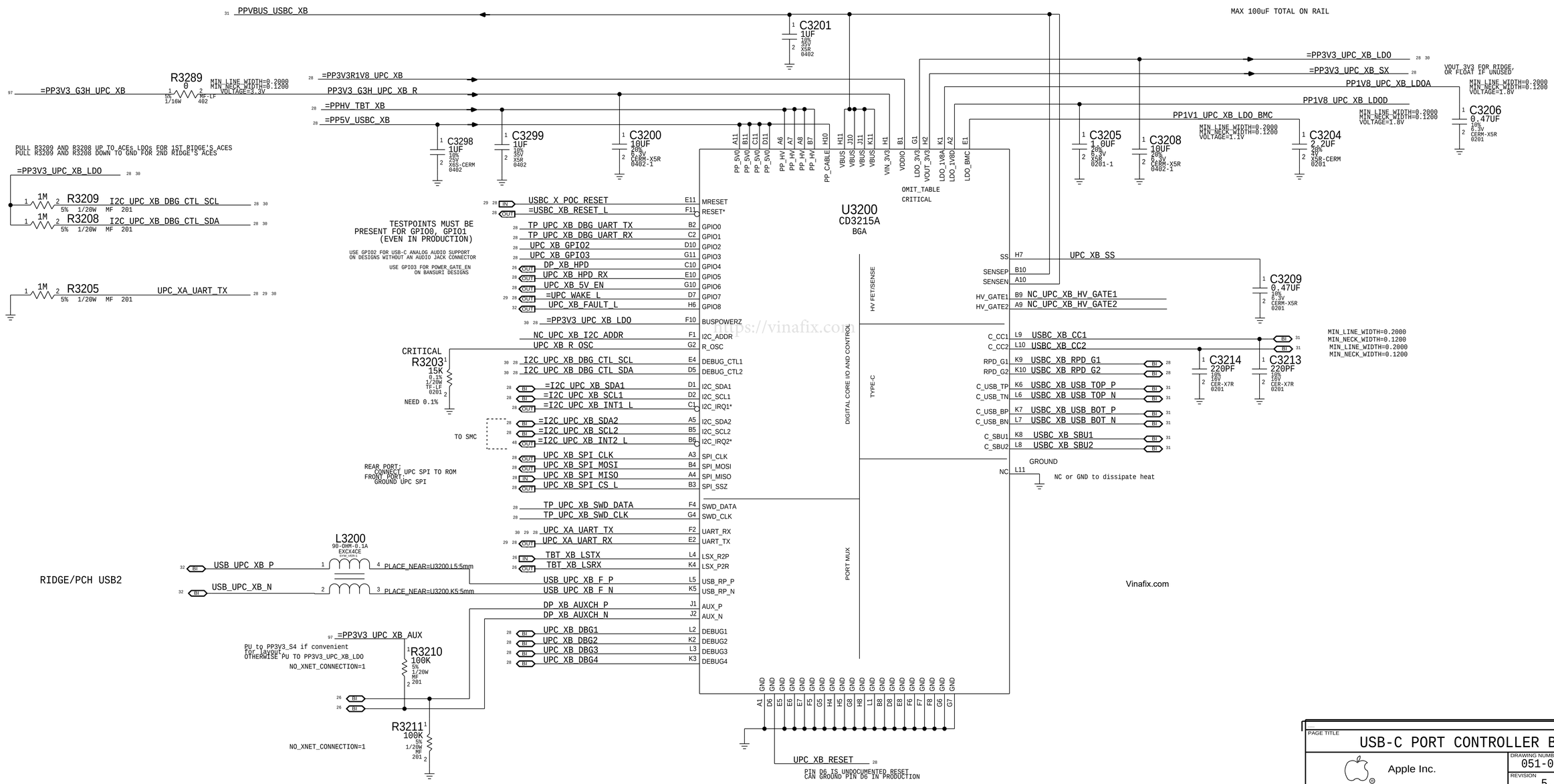
SECONDARY ACE USB-C PORT CONTROLLER (UPC)



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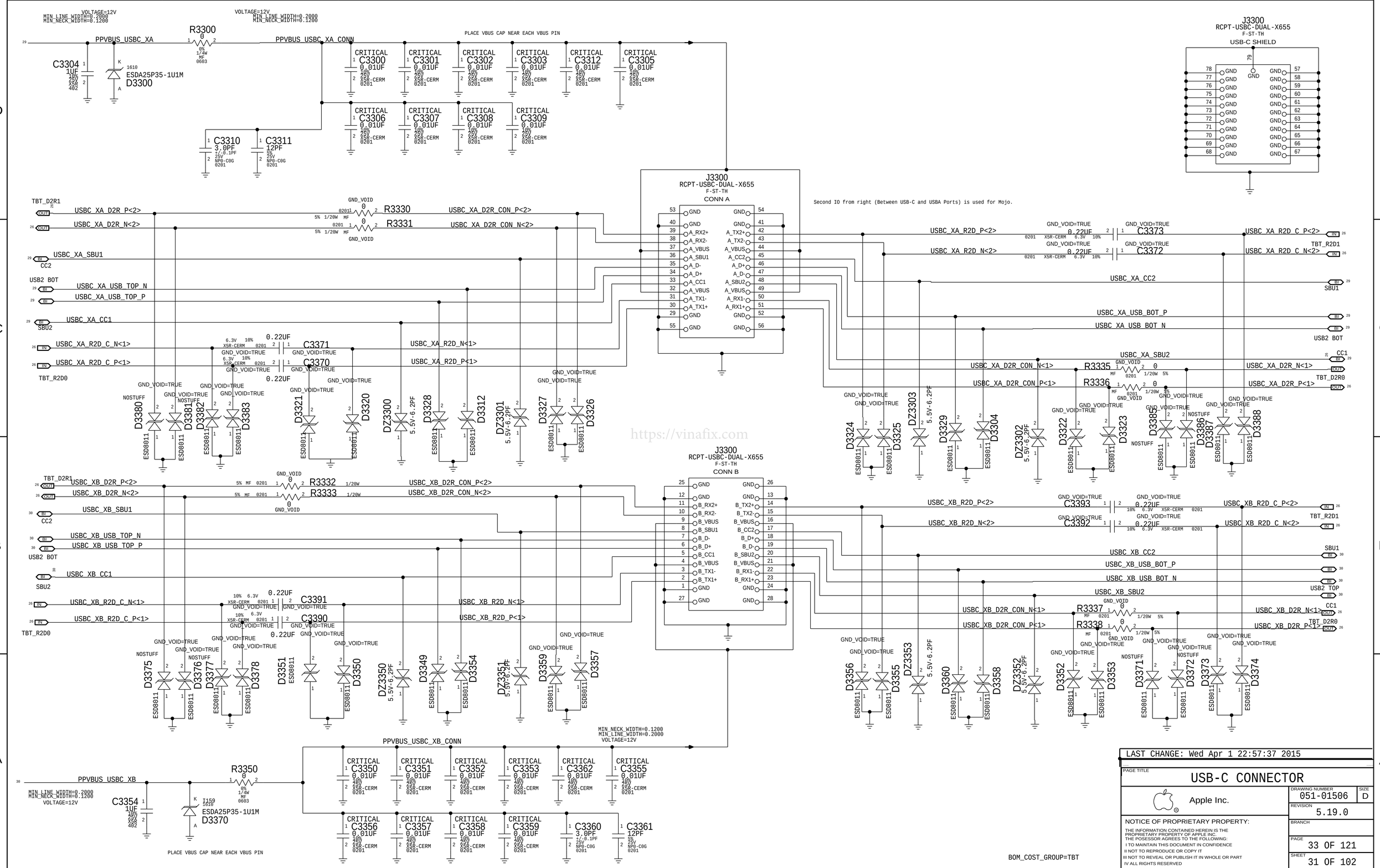

LAST CHANGE: Wed Apr 1 22:57:37 2015

PAGE TITLE
USB-C CONNECTOR

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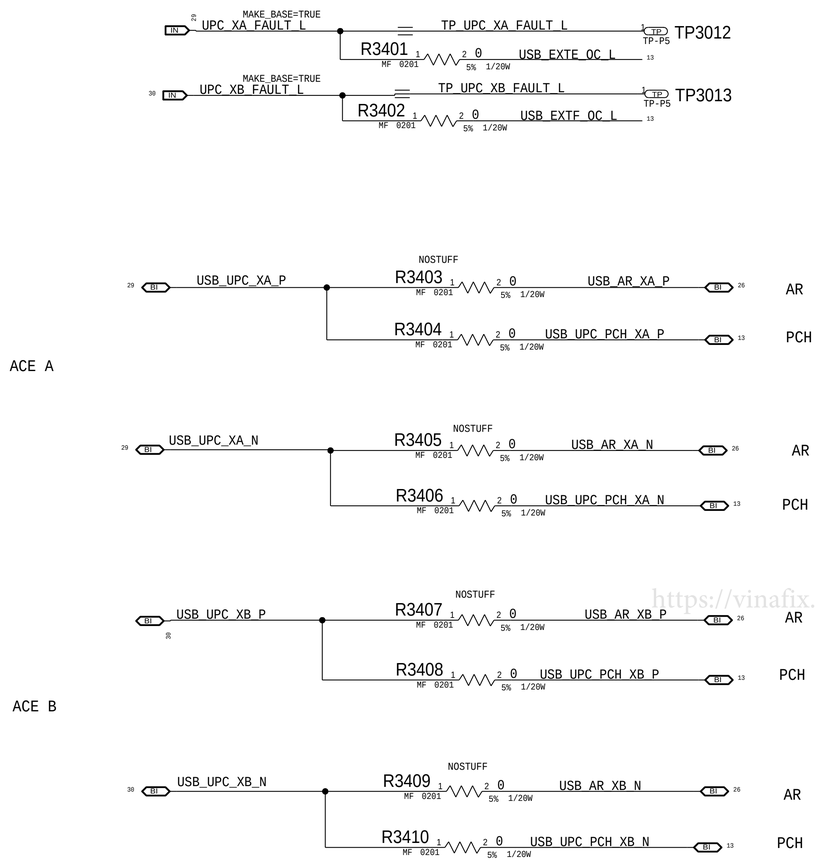

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BOM_COST_GROUP=USB-C

PAGE TITLE

USB-C Support 2

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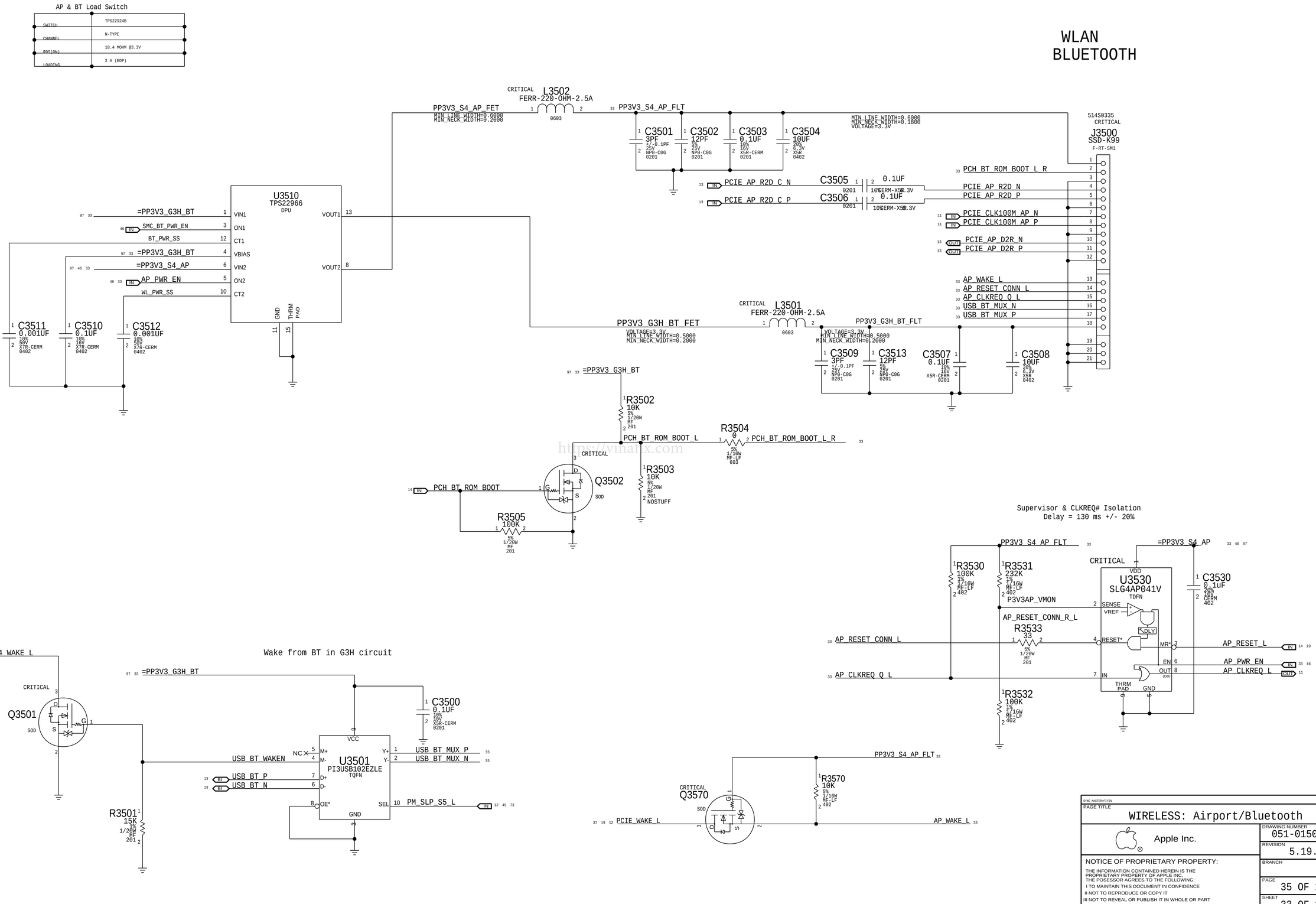
AP & BT Load Switch
SWITCH TPS22924B
CHANNEL N-TYPE
RDS(ON) 18.4 MOHM @3.3V
LOADING 2 A (EDP)
WLAN
BLUETOOTH
L3502 FERR-220-OHM-2.5A
PP3V3_S4_AP_FET
PP3V3_S4_AP_FLT
C3501 3PF
C3502 12PF
C3503 0.1UF
C3504 10UF
J3500 SSD-K99
514S0335 CRITICAL
PCH_BT_ROM_BOOT_L_R
PCIE_AP_R2D_N
PCIE_AP_R2D_P
C3505 0.1UF
C3506 0.1UF
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
PCIE_AP_D2R_N
PCIE_AP_D2R_P
AP_WAKE_L
AP_RESET_CONN_L
AP_CLKREQ_Q_L
USB_BT_MUX_N
USB_BT_MUX_P
U3510 TPS22966
=PP3V3_G3H_BT
SMC_BT_PWR_EN
BT_PWR_SS
=PP3V3_S4_AP
AP_PWR_EN
WL_PWR_SS
VIN1
ON1
CT1
VBIAS
VIN2
ON2
CT2
VOUT1
VOUT2
GND
THRM PAD
C3511 0.001UF
C3510 0.1UF
C3512 0.001UF
L3501 FERR-220-OHM-2.5A
PP3V3_G3H_BT_FET
PP3V3_G3H_BT_FLT
C3509 3PF
C3513 12PF
C3507 0.1UF
C3508 10UF
R3502 10K
R3504 0
R3503 10K
NOSTUFF
Q3502
PCH_BT_ROM_BOOT
R3505 100K
Supervisor & CLKREQ# Isolation
Delay = 130 ms +/- 20%
PP3V3_S4_AP_FLT
=PP3V3_S4_AP
R3530 100K
R3531 232K
P3V3AP_VMON
AP_RESET_CONN_R_L
R3533 33
R3532 100K
U3530 SLG4AP041V TDFN
C3530 0.1UF
AP_RESET_L
AP_PWR_EN
AP_CLKREQ_L
Wake from BT in G3H circuit
SMC_PME_S4_WAKE_L
Q3501
C3500 0.1UF
U3501 PI3USB102EZLE TQFN
USB_BT_WAKEN
USB_BT_P
USB_BT_N
PM_SLP_S5_L
R3501 15K
Q3570
R3570 10K
PCIE_WAKE_L
AP_WAKE_L
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WIRELESS: Airport/Bluetooth
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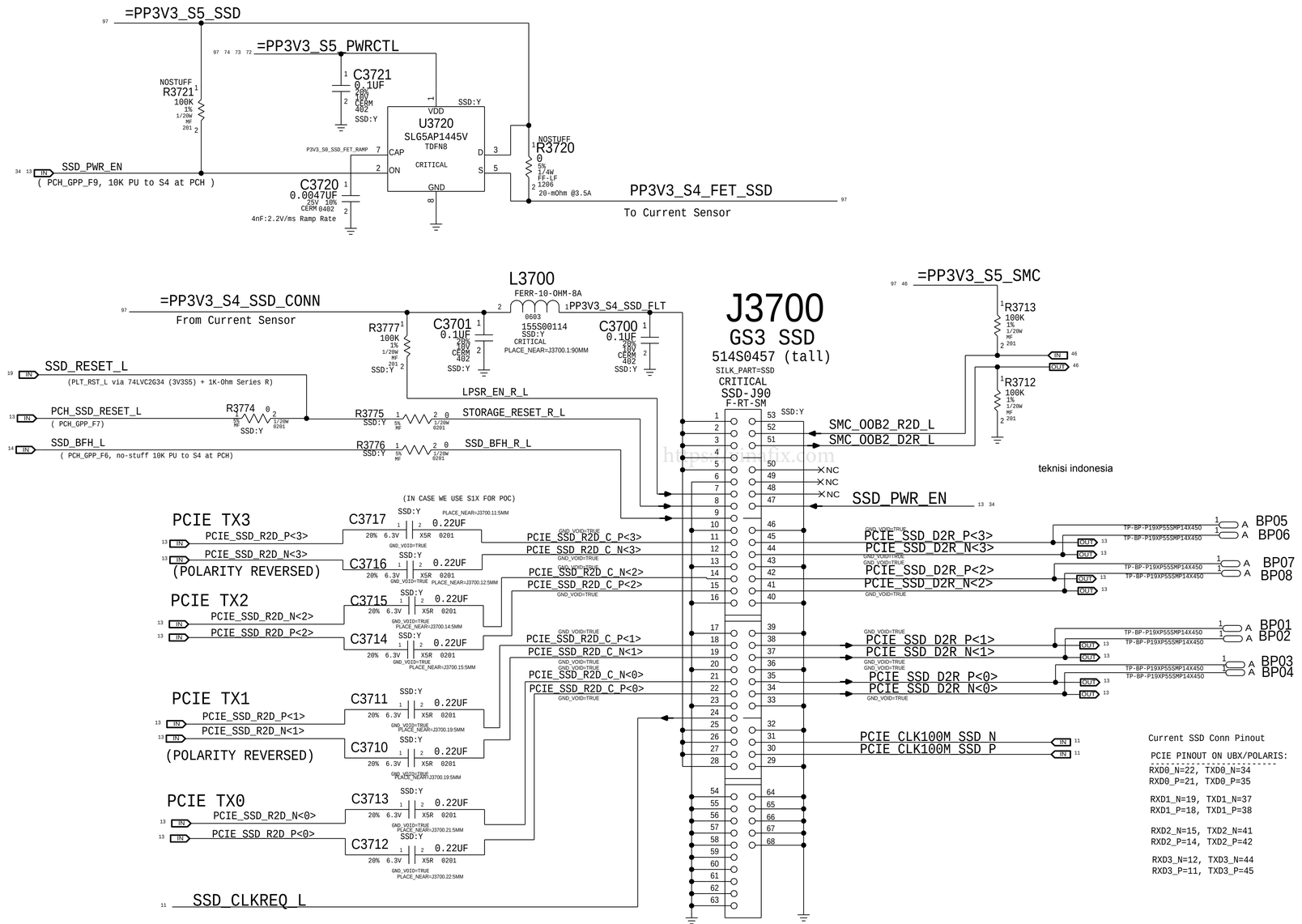

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SSD:CONNECTOR

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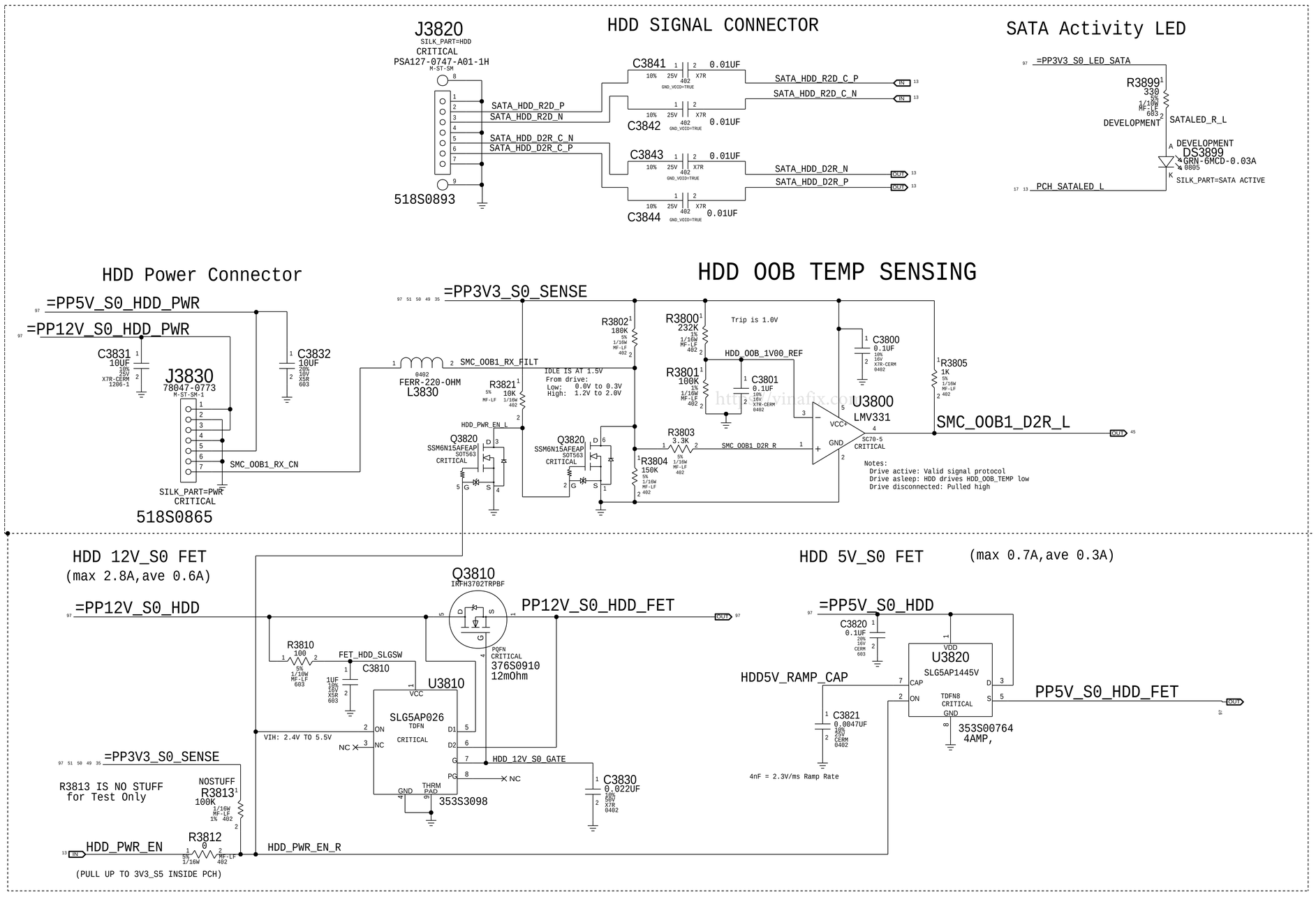

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HDD: CONN & Temp Sense

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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

97 37 36 =PP3V3_ENET_PHY
281mA (1000base-T max power, Caesar IV)

CRITICAL L3900 FERR-600-OHM-300MA-0.85OHM 0402 — MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V
C3900 0.1UF 10% 16V X5R-CERM 0201
ENET_XTALVDDH — MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V

CRITICAL L3905 FERR-600-OHM-300MA-0.85OHM 0402 — PP3V3_ENET_PHY_BIASVDDH — MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V
C3905 0.1UF 10% 16V X5R-CERM 0201

CRITICAL L3910 FERR-600-OHM-300MA-0.85OHM 0402 — PP3V3_ENET_PHY_AVDDH — MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V
R3910[1] 4.7K 5% 1/10W MF-LF 402
C3910 0.1UF 10% 16V X5R-CERM 0201
C3911 0.1UF 10% 16V X5R-CERM 0201

VDD for Card Reader I/O
37 =PP3V3R1V8_CR_VDDIO

ENET_SR_LX 37
=ENET_SR_VFB 37
Internal 1.2V Switching Regulator pins.

=PP1V2_ENET_PHY 37
396mA (1000base-T, Caesar II)

CRITICAL L3920 FERR-600-OHM-300MA-0.85OHM 0402 — PP1V2_ENET_PHY_AVDDL — MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.1500 VOLTAGE=1.2V
C3921 0.1UF 10% 16V X5R-CERM 0201
C3920 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL L3925 FERR-600-OHM-0.5A SM — PP1V2_ENET_PHY_PCIEPLL — MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=1.2V
C3926 0.1UF 10% 16V X5R-CERM 0201
C3925 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL L3930 FERR-600-OHM-300MA-0.85OHM 0402 — PP1V2_ENET_PHY_GPHYPLL — MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.1500 VOLTAGE=1.2V
C3931 0.1UF 10% 16V X5R-CERM 0201
C3930 4.7UF 20% 6.3V X5R-CERM1 402

C3936 0.1UF 10% 16V X5R-CERM 0201
C3935 10UF 20% 6.3V X5R 603

R3940[1] 4.7K 5% 1/10W MF-LF 402
[1]R3941 4.7K 5% 1/10W MF-LF 402
C3915 4.7UF 20% 6.3V X5R-CERM1 402
C3916 0.1UF 10% 16V X5R-CERM 0201

97 =PP3V3_S0_ENET
[1]R3942 1K 5% 1/10W MF-LF 402 — Current Limiting Resistor

C3950 0.1UF 10% 16V X5R-CERM 0201
C3951 0.1UF 10% 16V X5R-CERM 0201
C3955 0.1UF 10% 16V X5R-CERM 0201
C3956 0.1UF 10% 16V X5R-CERM 0201

13 OUT PCIE_ENET_D2R_N
13 OUT PCIE_ENET_D2R_P
13 IN PCIE_ENET_R2D_C_P
13 IN PCIE_ENET_R2D_C_N
37 OUT =ENET_WAKE_L
(See note)

WAKE#
Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

ENET_VMAIN_PRSNT
PCIE_ENET_D2R_C_N
PCIE_ENET_D2R_C_P
PCIE_ENET_R2D_P
PCIE_ENET_R2D_N
11 IN PCIE_CLK100M_ENET_P
11 IN PCIE_CLK100M_ENET_N
38 IN ENET_RESET_L
11 OUT ENET_CLKREQ_L
ENET_LOW_PWR
SMB_ENET_SCL
SMB_ENET_SDA
37 OUT ENET_TRAFFICLED_L
36 ENET_XTAL_IN
36 ENET_XTAL_OUT
ENET_RDAC

36 ENET_SCLK MF R3975 33 5% 1/20W MF 201 — ENET_SCLK_R
36 ENET_MISO_R MF R3976 33 5% 1/20W MF 201 — ENET_MISO
36 ENET_MOSI MF R3977 33 5% 1/20W MF 201 — ENET_MOSI_R
36 ENET_CS_L MF R3978 33 5% 1/20W MF 201 — ENET_CS_R_L

OMIT_TABLE
U3900
BCM57766C0KMLG
QFN-8X8

42 AVDDH, 48 AVDDH, 37 BIASVDDH, 17 XTALVDDH, 7, 20, 56, 62 VDDO, 14 SR_VDD, 15 SR_VDDP, 16 SR_LX, 13 SR_VFB, 39, 45, 51 AVDDL, 29 PCIE_PLLVDDL, 32, 36 GPHY_PLLVDDL, 35, 61 VDDC

58 VMAIN_PRSNT (IPD-ENET)
27 PCIE_TXD_N
28 PCIE_TXD_P
33 PCIE_RXD_P
34 PCIE_RXD_N
31 PCIE_REFCLK_P
30 PCIE_REFCLK_N
11 PERST* (IPD)
12 CLKREQ* (OD)
3 WAKE* (OD)
4 LOW_PWR (IPD)
6 SMB_CLK
10 SMB_DATA (IPD-ENETM)
66 SCLK_SPD1000LED* (IPU)
64 SI/EEDATA
65 SO_LINKLED*
63 CS*/EECLK
NC 2 SPD100LED*/SERIAL_DO (OD)
67 TRAFFICLED*/SERIAL_DI (OD)
18 XTALI
19 XTALO
38 RDAC
69 THRM_PAD

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

TRD0_P 40 — ENETCONN_MDI_P<0> — BI 37
TRD0_N 41 — ENETCONN_MDI_N<0> — BI 37
TRD1_P 44 — ENETCONN_MDI_P<1> — BI 37
TRD1_N 43 — ENETCONN_MDI_N<1> — BI 37
TRD2_P 46 — ENETCONN_MDI_P<2> — BI 37
TRD2_N 47 — ENETCONN_MDI_N<2> — BI 37
TRD3_P 50 — ENETCONN_MDI_N<3> — BI 37

PP3V3R1V8_ENET_LR_OUT 37 — MIN_LINE_WIDTH=0.3000 MIN_NECK_WIDTH=0.1500 VOLTAGE=3.3V

(IPD) GPIO_0/CR_ACT_LED* 5 — NC
GPIO_1/LR_OUT 8
GPIO_2/MEDIA_SENSE 9 — ENET_MEDIA_SENSE — OUT 14

NOTE: "IPx" == Programmable pull-up/down
SD_DETECT can only be used active low due to errata.

(IPx-ENET) SD_DETECT 1 — ENET_SD_DETECT_L — IN 38
(IPU-ENET) CR_CMD 26 — ENET_SD_CMD — R3961 33 5% 1/20W MF 201 — SDCONN_CMD — IN 38
CR_CLK 21 — ENET_SD_CLK — R3979 33 5% 1/20W MF 201 — SDCONN_CLK — OUT 38
(IPU-ENET)
CR_DATA0 25 — ENET_CR_DATA<0> — R3971 33 5% 1/20W MF 201 — SDCONN_DATA<0> — BI 38
CR_DATA1 24 — ENET_CR_DATA<1> — R3972 33 5% 1/20W MF 201 — SDCONN_DATA<1> — BI 38
CR_DATA2 23 — ENET_CR_DATA<2> — R3973 33 5% 1/20W MF 201 — SDCONN_DATA<2> — BI 38
CR_DATA3 22 — ENET_CR_DATA<3> — R3974 33 5% 1/20W MF 201 — SDCONN_DATA<3> — BI 38
CR_DATA4 52 — NC
CR_DATA5 53 — NC
CR_DATA6 54 — NC
CR_DATA7 55 — NC

No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.

(IPU-ENET) MS_INS* 59 — NC
(IPU-ENET) CR_LED*/CR_BUS_PWR 60 — ENET_CR_PWREN — OUT 38
(IPU-ENET) CR_WP* 57 — SDCONN_WP — IN 38
(NO IPU OR IPD-ENET) SR_DISABLE 68 — ENET_SR_DISABLE — R3981 1K 5% 1/16W MF-LF 402
(See note)

ENET 1.2V SR IS ENABLED IF FLOATING.

ENET_SR_DISABLE
If ENET switching regulator is used, this pin should have a 1K pull-down to GND

ENET supports both active-levels for WP.

ENET_CR Signals
BCM requests SD CR[0:7], CMD, CLK termination.

[1]R3965 1.24K 1% 1/16W MF-LF 402

PLACEMENT_NOTE=PLACE R3961 NEAR U3900
PLACEMENT_NOTE=PLACE R3979 NEAR U3900
PLACEMENT_NOTE=PLACE R3971 NEAR U3900
PLACEMENT_NOTE=PLACE R3972 NEAR U3900
PLACEMENT_NOTE=PLACE R3973 NEAR U3900
PLACEMENT_NOTE=PLACE R3974 NEAR U3900

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy.
Avoids need for EFI to program at startup.
(Required ROM size 1 Mbit)

97 37 36 =PP3V3_ENET_PHY
C3990 0.1UF 10% 16V X5R-CERM 0201
U3990 AT45DB011D SOIC-8S1 OMIT_TABLE
VCC 6, SCK 2, CS* 4, WP* 5, RESET* 3, GND 7, SI 1, SO 8
36 ENET_SCLK
36 ENET_CS_L
ENET_MOSI 36
ENET_MISO_R 36
NOSTUFF [1]R3990 4.7K 5% 1/16W MF-LF 402
[1]R3997 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

Ethernet 25MHz Crystal

C3945 20PF 5% 50V CERM 0402
C3946 20PF 5% 50V CERM 0402
ENET_XTAL_OUT_R — R3945 0 5% 1/16W MF-LF 402 — ENET_XTAL_OUT 36
NOSTUFF R3946 1M 5% 1/16W MF-LF 402
CRITICAL Y3900 25.000MHZ-20PPM-12PF-85C 3.2X2.5MM-SM PLACE_NEAR=U3900.18:10MM
NC NC
ENET_XTAL_IN 36
NOTE: 30 PPM crystal required

BOM_COST_GROUP=ETHERNET

SYNC_MASTER=FIYIN SYNC_DATE=01/19/2010
PAGE TITLE
ETHERNET: PHY (CAESAR IV)

Apple Inc.

DRAWING NUMBER	SIZE
051-01506	D
REVISION 5.19.0	
BRANCH	
PAGE 39 OF 121	
SHEET 36 OF 102	

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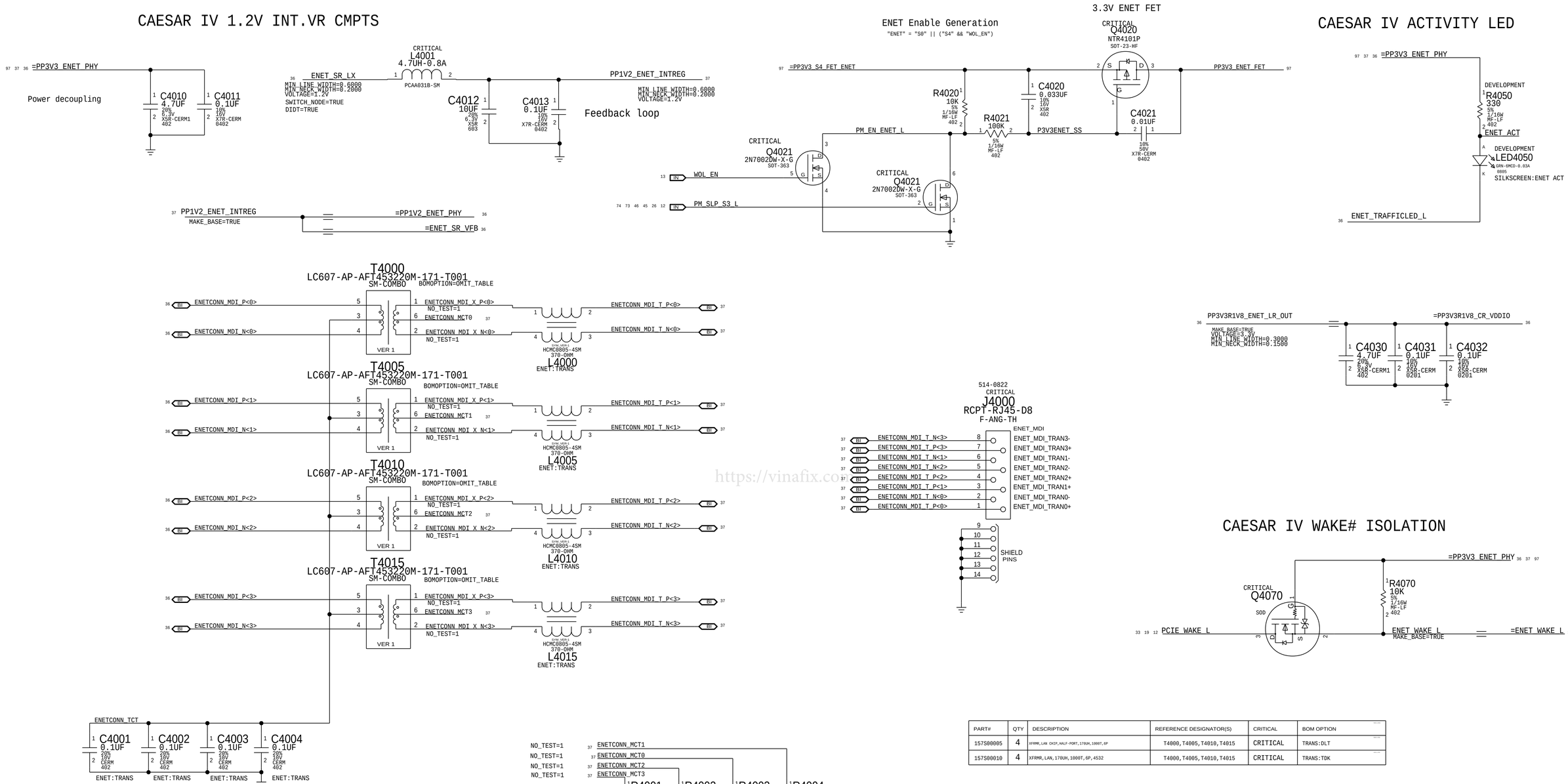

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
157S00005	4	XFRMR,LAN CHIP,HALF-PORT,170UH,1000T,6P	T4000,T4005,T4010,T4015	CRITICAL	TRANS:DLT
157S00010	4	XFRMR,LAN,170UH,1000T,6P,4532	T4000,T4005,T4010,T4015	CRITICAL	TRANS:TDK

BOM_COST_GROUP=ETHERNET

PAGE TITLE
ETHERNET: Support & Connector

Apple Inc.

DRAWING NUMBER 051-01506
SIZE D
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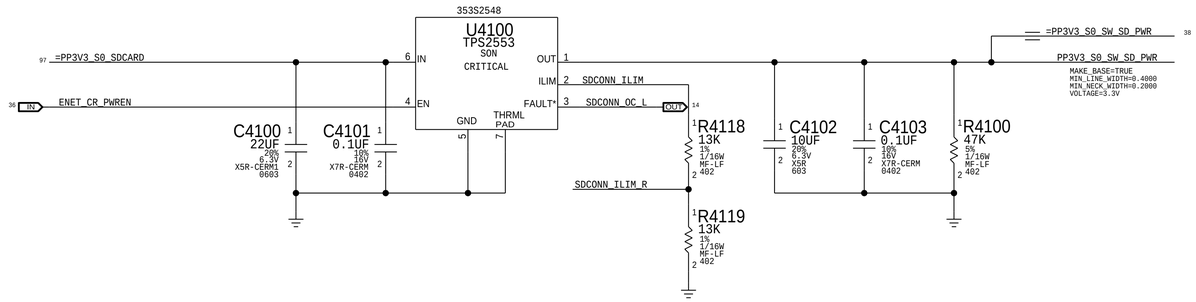
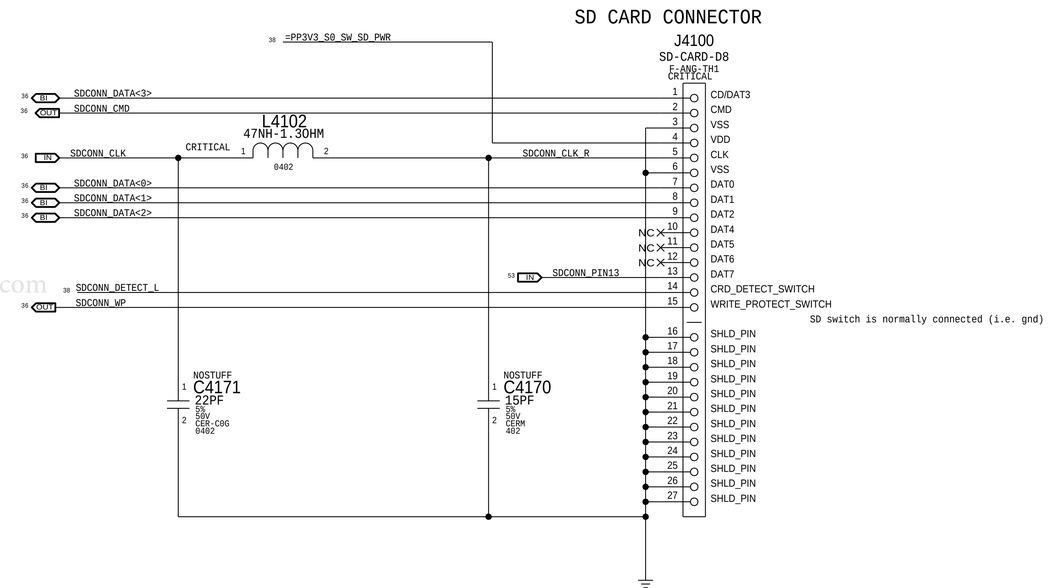
SD CARD 3.3V OVERCURRENT PROTECTION CHIP



J16:516-0249 / J17:512-0038

SD CARD CONNECTOR



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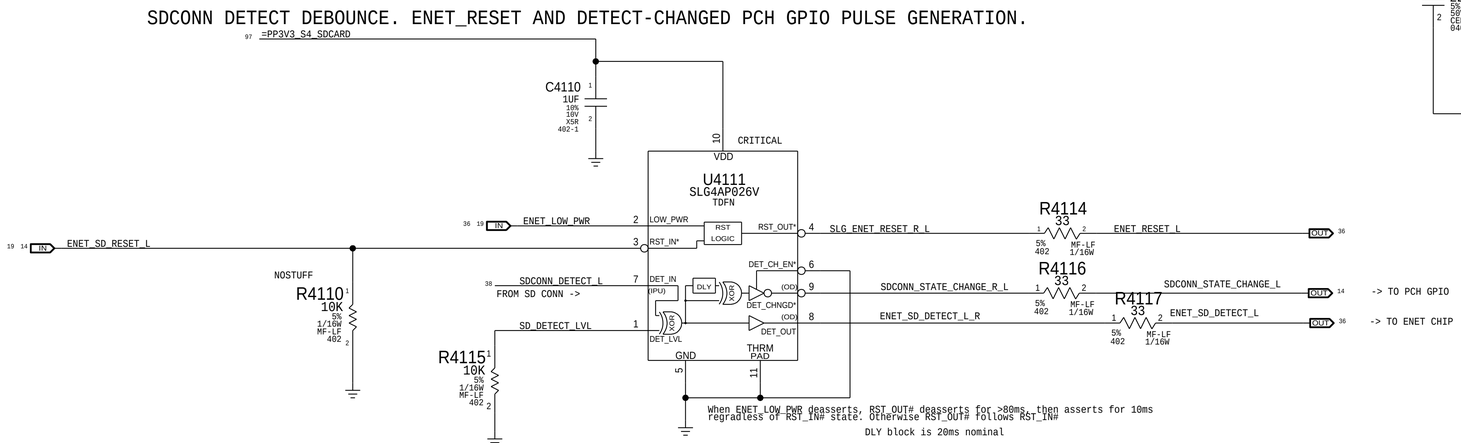
SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.



BOM_COST_GROUP=SD CARD

SYNC_MASTER=FIYIN SYNC_DATE=01/19/2016

PAGE TITLE

SD CARD: Connector

Apple Inc.

DRAWING NUMBER 051-01506 SIZE D

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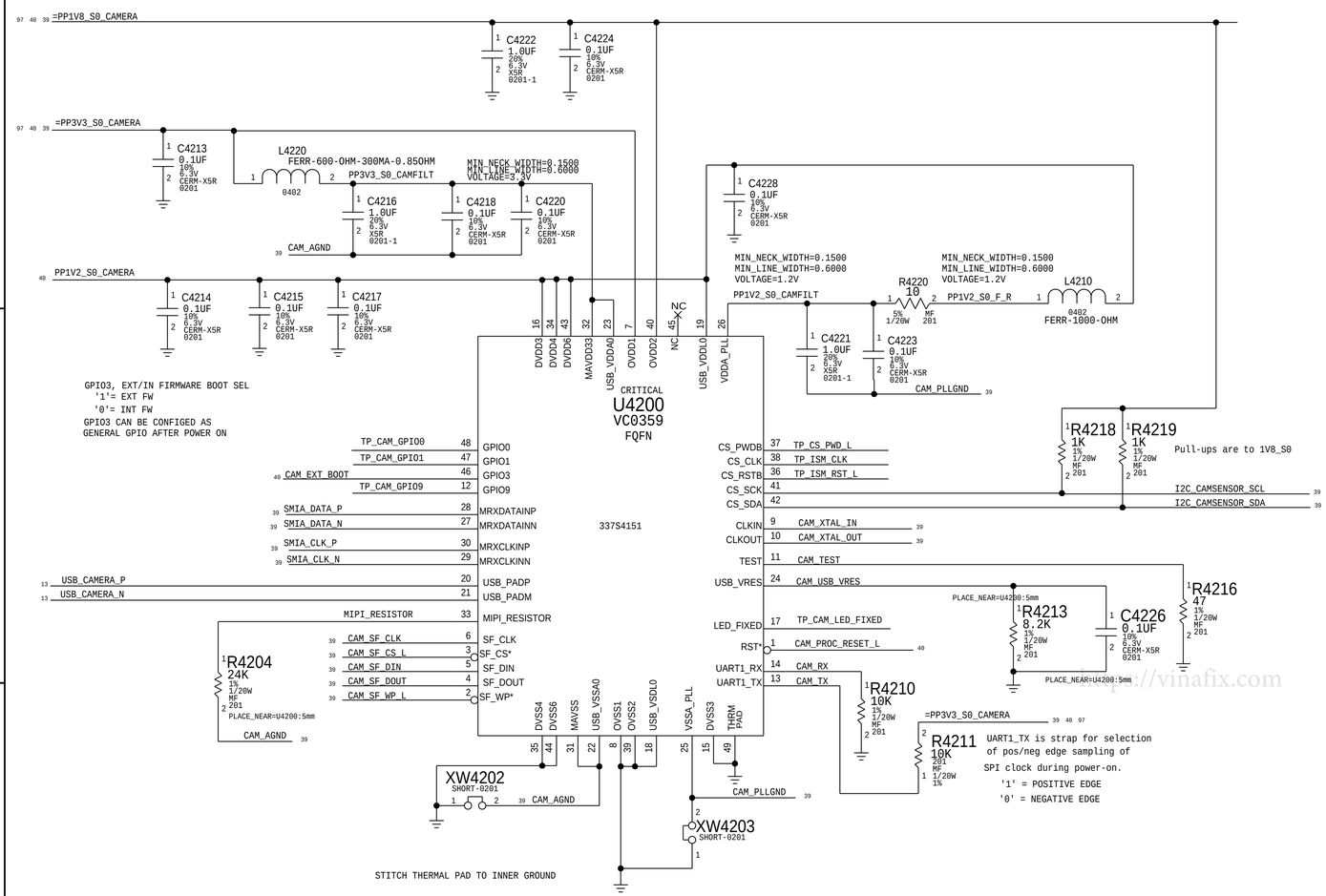
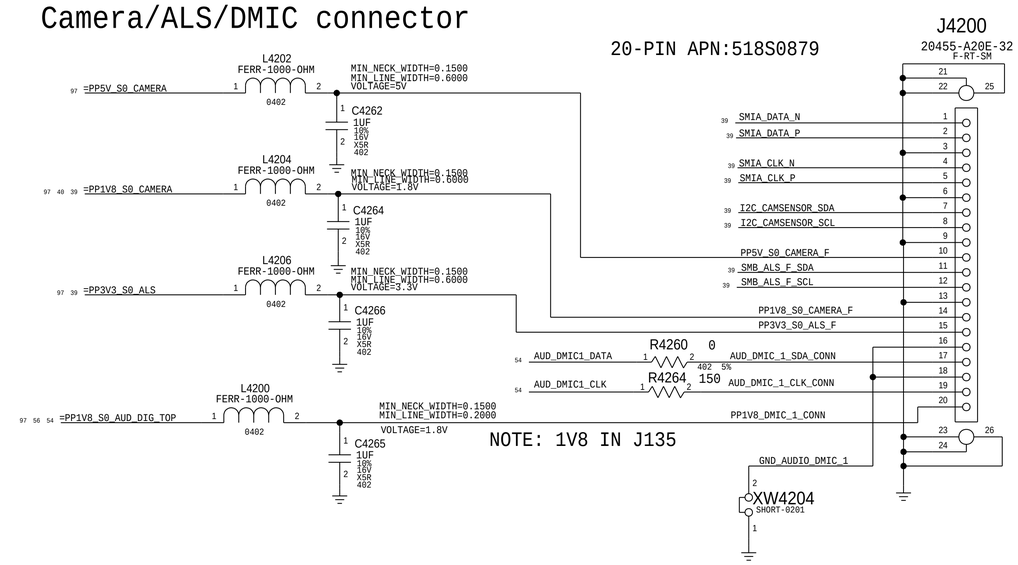
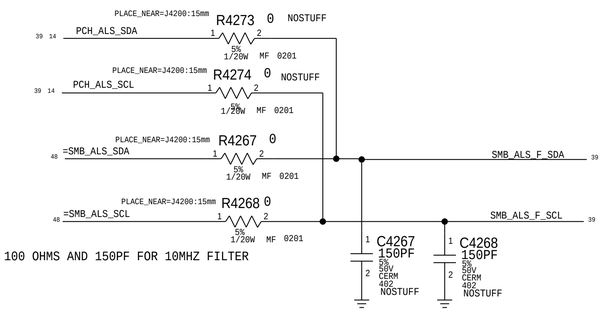
USB CAMERA CONTROLLER

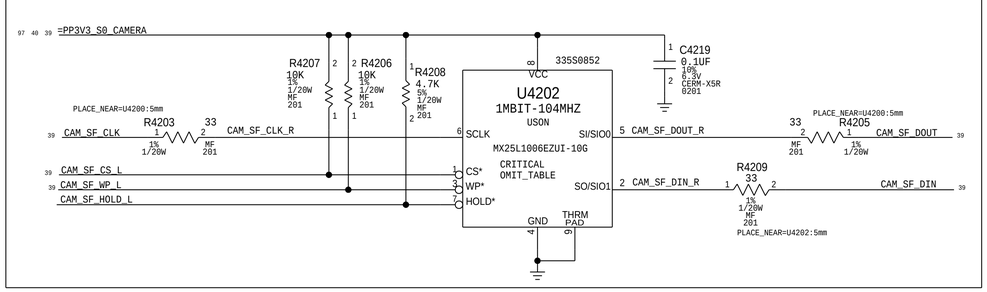


Camera/ALS/DMIC connector

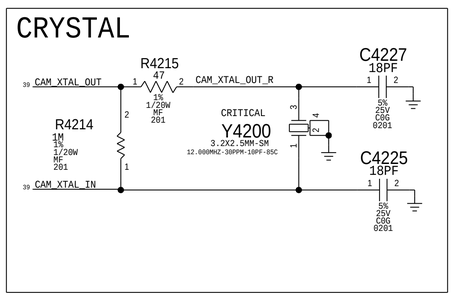




SERIAL FLASH

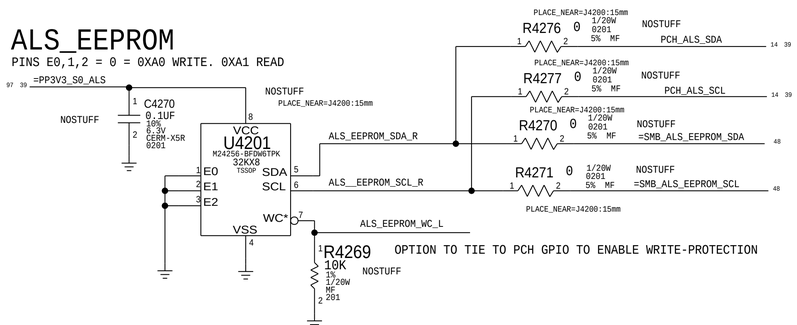


CRYSTAL



ALS_EEPROM

PINS E0,1,2 = 0 = 0XA0 WRITE. 0XA1 READ



BOM_COST_GROUP=CAMERA

PAGE TITLE	CAMERA: Controller
Apple Inc.	DRAWING NUMBER 051-01506 SIZE D
	REVISION 5.19.0
	BRANCH
	PAGE 42 OF 121
	SHEET 39 OF 102

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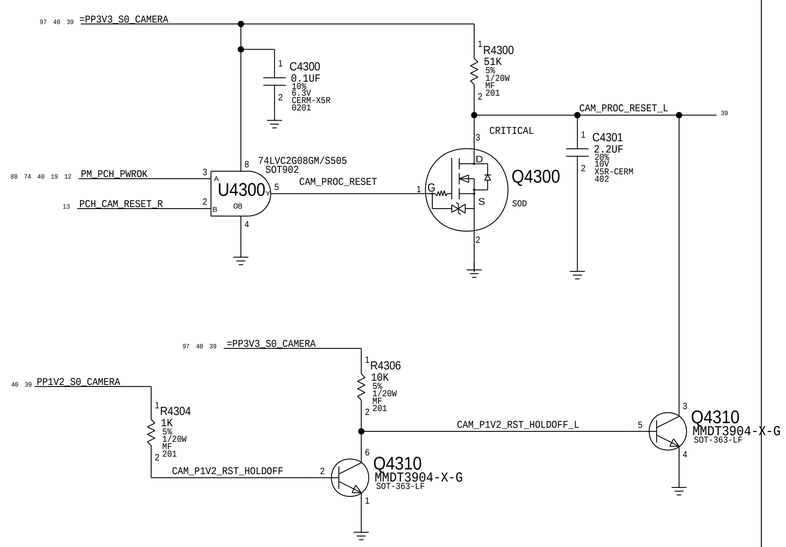
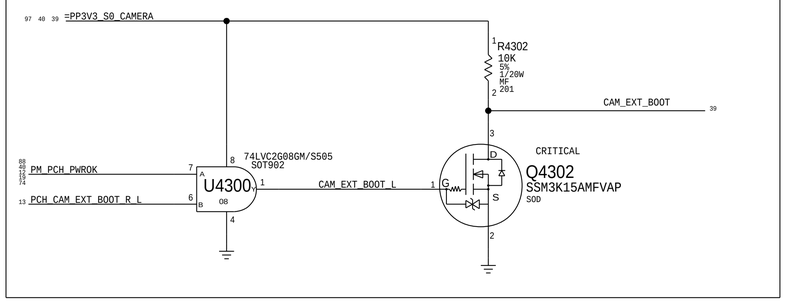
Camera Processor Reset



Camera Processor ExtBoot Cntl



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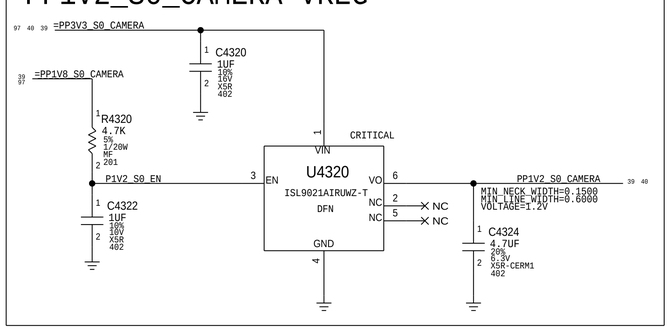
PP1V2_S0_CAMERA VREG



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BOM_COST_GROUP=CAMERA

SYNC_MASTER=DDRESSLER	SYNC_DATE=08/27/2016
PAGE TITLE: CAMERA: Controller Support	
Apple Inc.	DRAWING NUMBER: 051-01506 / SIZE: D
	REVISION: 5.19.0
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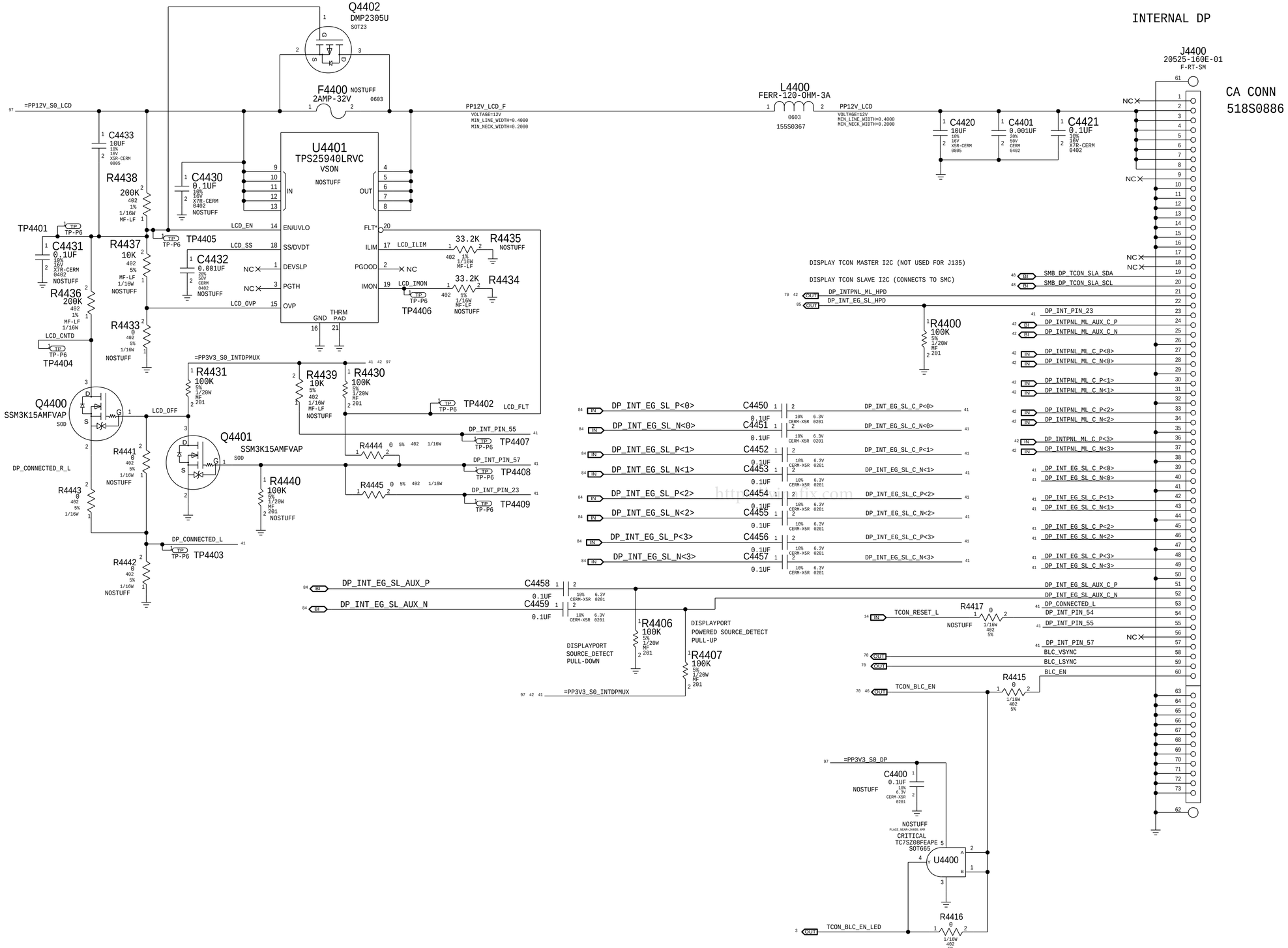
	PAGE: 43 OF 121
	SHEET: 40 OF 102



SYNC_MASTER=ANDREW SYNC_DATE=10/04/2010

PAGE TITLE

DISPLAY: Support

Apple Inc.

DRAWING NUMBER 051-01506 SIZE D

REVISION 5.19.0

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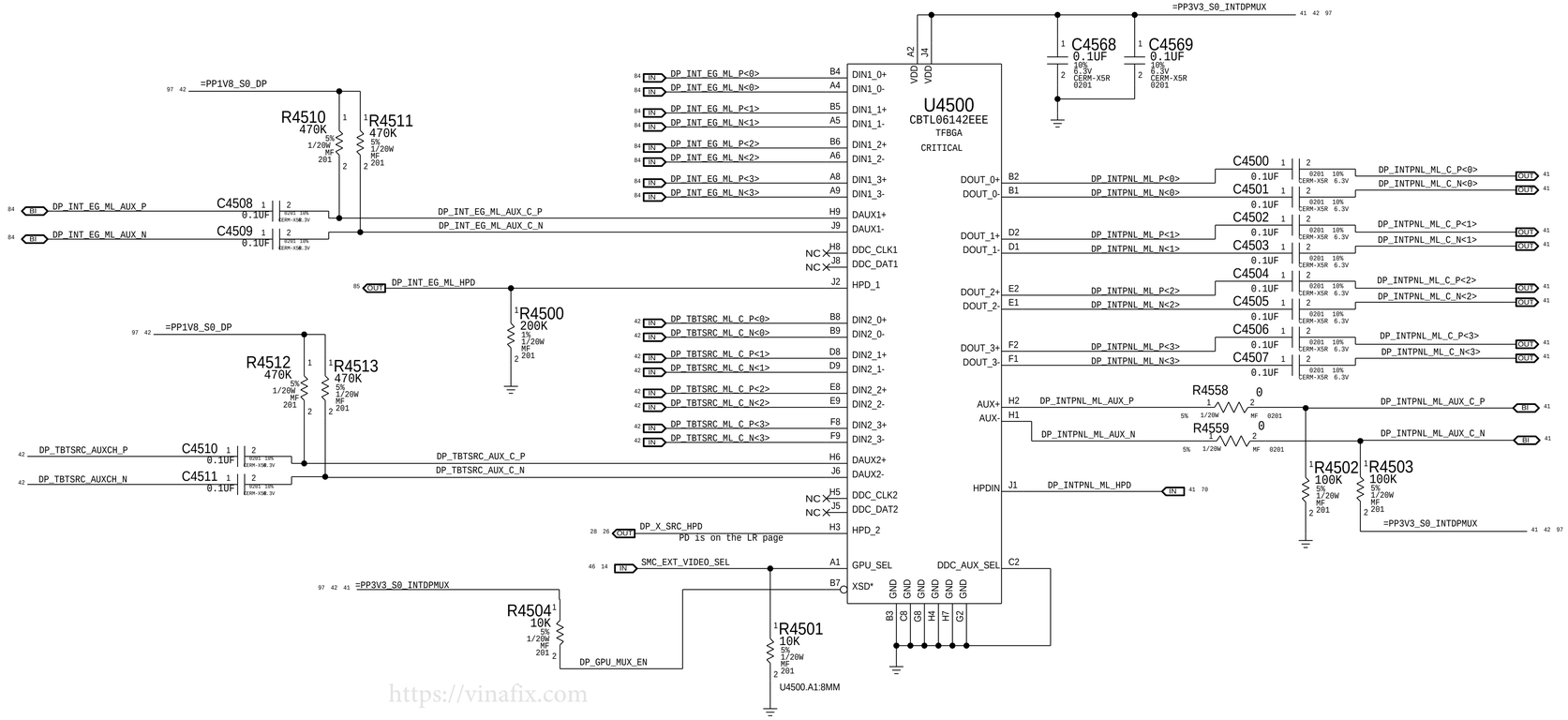
TP to DP aliases

26 IN	DP_X_SRC_ML_P<0>	DP_TBTSRC_ML_P<0>	42
26 IN	DP_X_SRC_ML_N<0>	DP_TBTSRC_ML_N<0>	42
26 IN	DP_X_SRC_ML_P<1>	DP_TBTSRC_ML_P<1>	42
26 IN	DP_X_SRC_ML_N<1>	DP_TBTSRC_ML_N<1>	42
26 IN	DP_X_SRC_ML_P<2>	DP_TBTSRC_ML_P<2>	42
26 IN	DP_X_SRC_ML_N<2>	DP_TBTSRC_ML_N<2>	42
26 IN	DP_X_SRC_ML_P<3>	DP_TBTSRC_ML_P<3>	42
26 IN	DP_X_SRC_ML_N<3>	DP_TBTSRC_ML_N<3>	42
26 BI	DP_X_SRC_AUX_P	DP_TBTSRC_AUXCH_P	42
26 BI	DP_X_SRC_AUX_N	DP_TBTSRC_AUXCH_N	42



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42 IN	DP_TBTSRC_ML_P<0>	DP_TBTSRC_ML_C_P<0>	42
42 IN	DP_TBTSRC_ML_N<0>	DP_TBTSRC_ML_C_N<0>	42
42 IN	DP_TBTSRC_ML_P<1>	DP_TBTSRC_ML_C_P<1>	42
42 IN	DP_TBTSRC_ML_N<1>	DP_TBTSRC_ML_C_N<1>	42
42 IN	DP_TBTSRC_ML_P<2>	DP_TBTSRC_ML_C_P<2>	42
42 IN	DP_TBTSRC_ML_N<2>	DP_TBTSRC_ML_C_N<2>	42
42 IN	DP_TBTSRC_ML_P<3>	DP_TBTSRC_ML_C_P<3>	42
42 IN	DP_TBTSRC_ML_N<3>	DP_TBTSRC_ML_C_N<3>	42

BOM_COST_GROUP=DISPLAY

SYNC_MASTER=ANDREW SYNC_DATE=02/17/2016

PAGE TITLE
DISPLAY: MUXing

Apple Inc.

DRAWING NUMBER 051-01506 SIZE D

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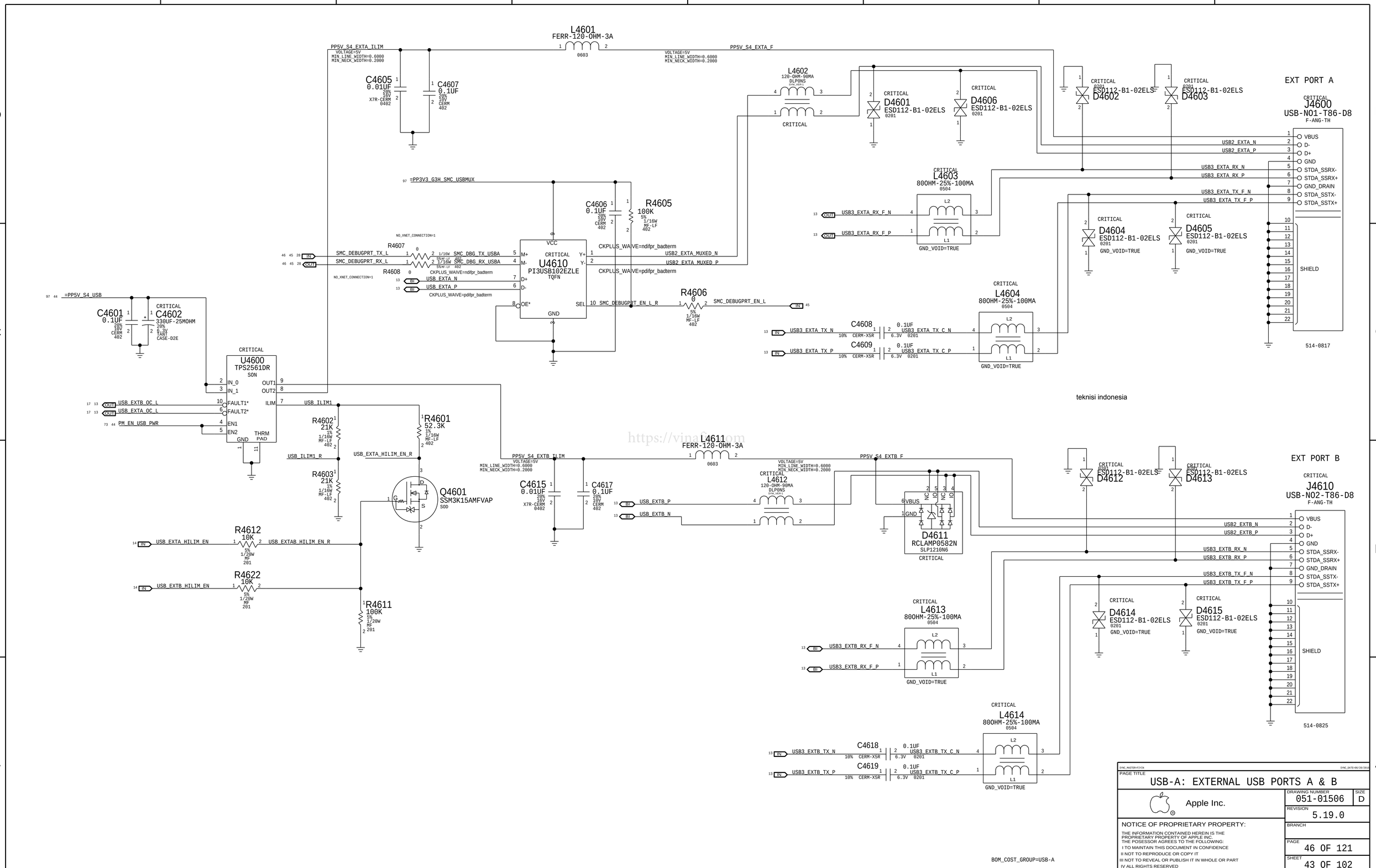
L4601
FERR-120-OHM-3A
0603
PP5V_S4_EXTA_ILIM
PP5V_S4_EXTA_F
VOLTAGE=5V
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
C4605
0.01UF
20%
16V
X7R-CERM
0402
C4607
0.1UF
20%
10V
CERM
402
L4602
120-OHM-90MA
DLP0NS
CRITICAL
D4601
ESD112-B1-02ELS
0201
D4606
ESD112-B1-02ELS
0201
D4602
ESD112-B1-02ELS
0201
D4603
ESD112-B1-02ELS
0201
EXT PORT A
J4600
USB-N01-T86-D8
F-ANG-TH
VBUS
D-
D+
GND
STDA_SSRX-
STDA_SSRX+
GND_DRAIN
STDA_SSTX-
STDA_SSTX+
SHIELD
514-0817
USB2_EXTA_N
USB2_EXTA_P
USB3_EXTA_RX_N
USB3_EXTA_RX_P
USB3_EXTA_TX_F_N
USB3_EXTA_TX_F_P
=PP3V3_G3H_SMC_USBMUX
C4606
0.1UF
R4605
100K
5%
1/16W
MF-LF
402
R4607
R4608
SMC_DEBUGPRT_TX_L
SMC_DEBUGPRT_RX_L
SMC_DBG_TX_USBA
SMC_DBG_RX_USBA
NO_XNET_CONNECTION=1
U4610
PI3USB102ZLE
TQFN
VCC
GND
M+
M-
D+
D-
OE*
Y+
Y-
SEL
USB_EXTA_N
USB_EXTA_P
CKPLUS_WAIVE=ndifpr_badterm
CKPLUS_WAIVE=pdifpr_badterm
USB2_EXTA_MUXED_N
USB2_EXTA_MUXED_P
SMC_DEBUGPRT_EN_L_R
R4606
SMC_DEBUGPRT_EN_L
L4603
800HM-25%-100MA
0504
L2
L1
GND_VOID=TRUE
D4604
ESD112-B1-02ELS
0201
D4605
ESD112-B1-02ELS
0201
L4604
800HM-25%-100MA
0504
C4608
C4609
0.1UF
USB3_EXTA_TX_C_N
USB3_EXTA_TX_C_P
=PP5V_S4_USB
C4601
0.1UF
C4602
330UF-25MOHM
20%
0.3V
TANT
CASE-D2E
U4600
TPS2561DR
SON
IN_0
IN_1
OUT1
OUT2
FAULT1*
FAULT2*
EN1
EN2
ILIM
GND
THRM PAD
USB_EXTB_OC_L
USB_EXTA_OC_L
PM_EN_USB_PWR
USB_ILIM1
R4602
21K
1%
1/16W
MF-LF
402
R4601
52.3K
1%
USB_ILIM1_R
R4603
USB_EXTA_HILIM_EN_R
Q4601
SSM3K15AMFVAP
SOD
R4612
10K
USB_EXTA_HILIM_EN
USB_EXTAB_HILIM_EN_R
R4622
USB_EXTB_HILIM_EN
R4611
100K
L4611
FERR-120-OHM-3A
PP5V_S4_EXTB_ILIM
PP5V_S4_EXTB_F
C4615
0.01UF
C4617
0.1UF
L4612
120-OHM-90MA
DLP0NS
USB_EXTB_P
USB_EXTB_N
D4611
RCLAMP0582N
SLP1210N6
VBUS
GND
D4612
ESD112-B1-02ELS
0201
D4613
ESD112-B1-02ELS
0201
EXT PORT B
J4610
USB-N02-T86-D8
F-ANG-TH
USB2_EXTB_N
USB2_EXTB_P
USB3_EXTB_RX_N
USB3_EXTB_RX_P
USB3_EXTB_TX_F_N
USB3_EXTB_TX_F_P
L4613
800HM-25%-100MA
0504
D4614
ESD112-B1-02ELS
0201
D4615
ESD112-B1-02ELS
0201
514-0825
L4614
800HM-25%-100MA
0504
C4618
C4619
USB3_EXTB_TX_C_N
USB3_EXTB_TX_C_P
BOM_COST_GROUP=USB-A
PAGE TITLE
USB-A: EXTERNAL USB PORTS A & B
Apple Inc.
DRAWING NUMBER
051-01506
SIZE
D
REVISION
5.19.0
BRANCH
PAGE
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43 OF 102
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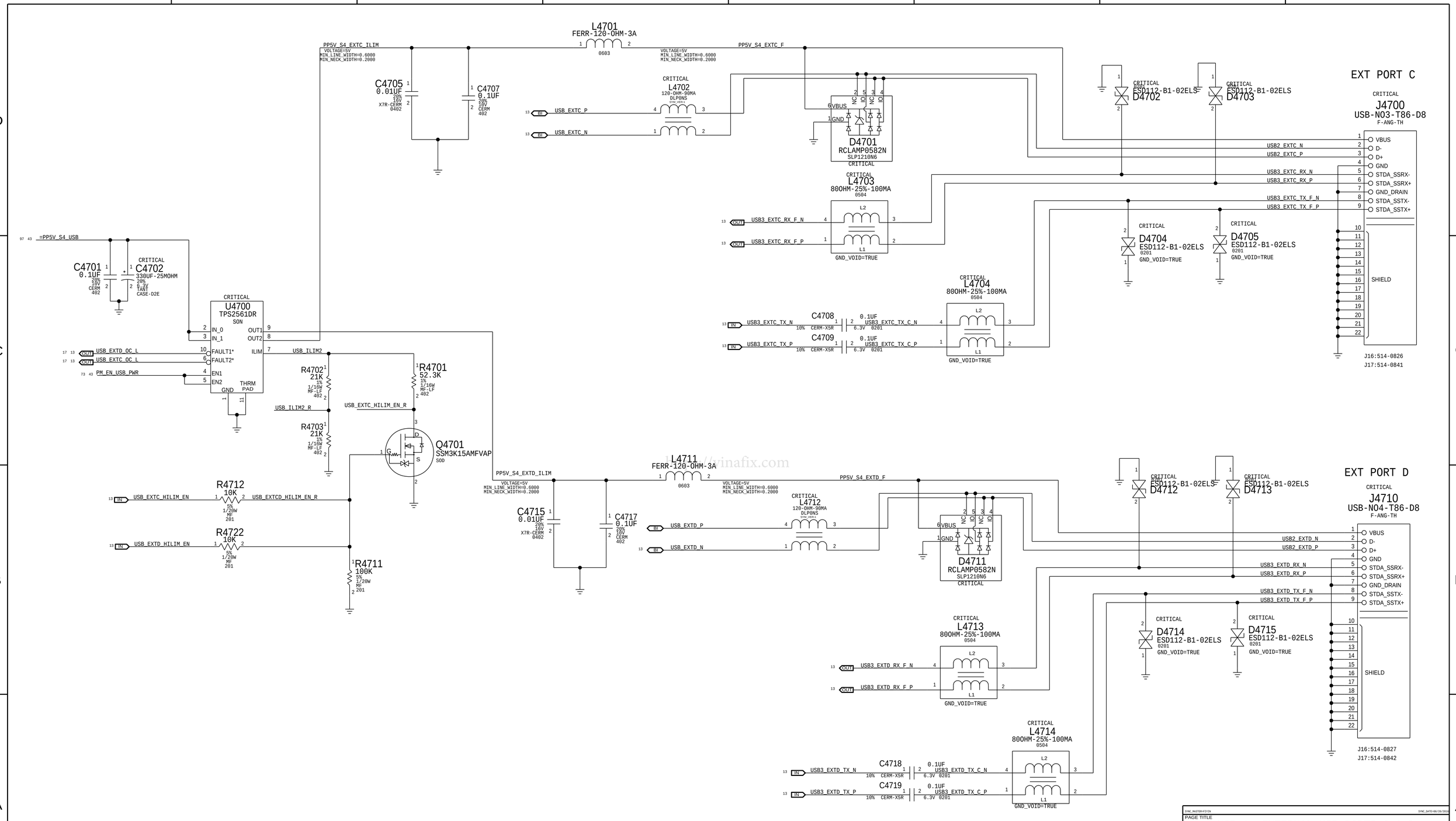

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SYNC_MASTER=F21DX SYNC_DATE=06/28/2016

PAGE TITLE

USB-A: EXTERNAL USB PORTS C & D

Apple Inc.

DRAWING NUMBER 051-01506 SIZE D

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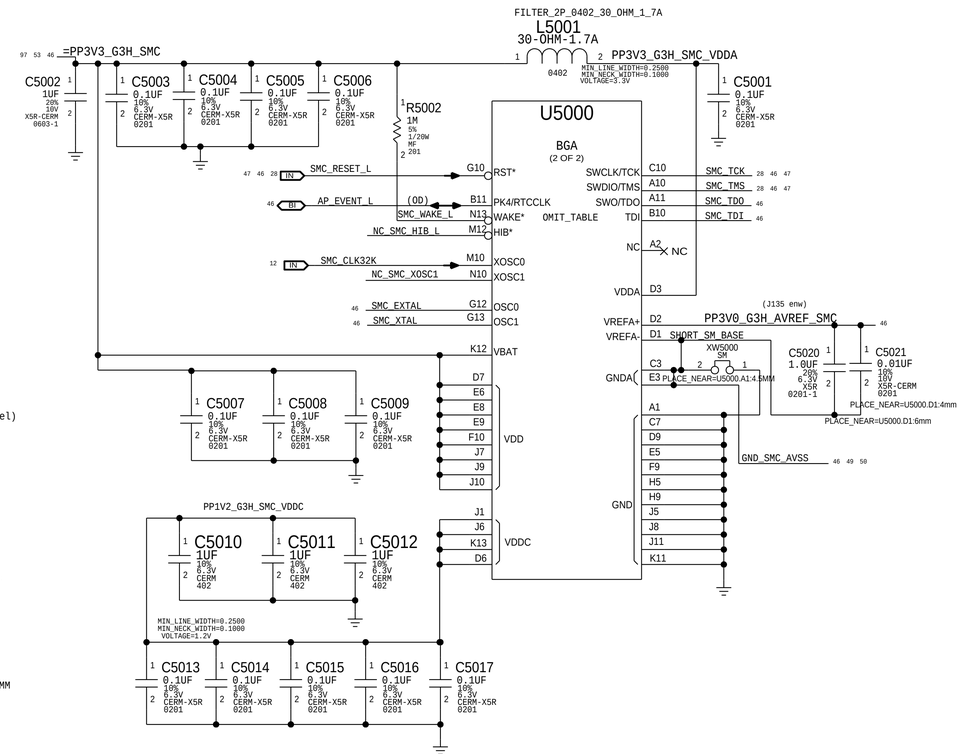
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

APN IN BOM PAGE:
338S1214-A-TI (LM4FS1EH5BB)

U5000
BGA
(1 OF 2)
OMIT_TABLE

Net	Dir	Pin	Pin name	Attr	Net	Dir	Pin	Pin name	Attr
LPC_AD<0>	BI	B13	LPC0AD0	arch	SMC_ADC0	IN	E2	AIN00	proj analog
LPC_AD<1>	BI	A13	LPC0AD1	arch	SMC_ADC1	IN	E1	AIN01	proj analog
LPC_AD<2>	BI	C12	LPC0AD2	arch	SMC_ADC2	IN	F2	AIN02	proj analog
LPC_AD<3>	BI	D11	LPC0AD3	arch	SMC_ADC3	IN	F1	AIN03	proj analog
LPC_CLK24M_SMC	IN	H12	LPC0CLK	arch	SMC_ADC4	IN	B3	AIN04	proj analog
LPC_FRAME_L	IN	D12	LPC0FRAME*	arch	SMC_ADC5	IN	A3	AIN05	proj analog
SMC_LRESET_L	IN	C13	LPC0RESET*	arch	SMC_ADC6	IN	B4	AIN06	proj analog
LPC_SERIRQ	BI	H13	LPC0SERIRQ	arch od	SMC_ADC7	IN	A4	AIN07	proj analog
PM_CLKRUN_L	OUT	G11	LPC0CLKRUN*	arch od	SMC_ADC8	IN	B5	AIN08	proj analog
LPC_PWRDWN_L	IN	F13	LPC0PD*	arch	SMC_ADC9	IN	A5	AIN09	proj analog
SMC_RUNTIME_SCI_L	OUT	F12	LPC0SCI*	arch	SMC_ADC10	IN	B6	AIN10	proj analog
SMC_WAKE_SCI_L	OUT	B12	PK5	arch	SMC_ADC11	IN	A6	AIN11	proj analog
					SMC_ADC12	IN	C1	AIN12	proj analog
					SMC_ADC13	IN	C2	AIN13	proj analog
					SMC_ADC14	IN	B1	AIN14	proj analog
					SMC_ADC15	IN	B2	AIN15	proj analog
					SMC_ADC16	IN	G2	AIN16	proj analog
					SMC_ADC17	IN	G1	AIN17	proj analog
					SMC_ADC18	IN	H1	AIN18	proj analog
					SMC_ADC19	IN	H2	AIN19	proj analog
					SMC_ADC20	IN	B7	AIN20	proj analog
					SMC_ADC21	IN	A7	AIN21	proj analog
					SMC_ADC22	IN	B8	AIN22	proj analog
					SMC_ADC23	IN	A8	AIN23	proj analog
SMBUS_SMC_0_S0_SCL	BI	E10	I2C0SCL	arch od					
SMBUS_SMC_0_S0_SDA	BI	D13	I2C0SDA	arch od					
SMBUS_SMC_1_S0_SCL	BI	M4	I2C1SCL	arch od					
SMBUS_SMC_1_S0_SDA	BI	N2	I2C1SDA	arch od					
SMBUS_SMC_2_S0_SCL	BI	N8	I2C2SCL	arch od					
SMBUS_SMC_2_S0_SDA	BI	M8	I2C2SDA	arch od					
SMBUS_SMC_3_SCL	BI	L8	I2C3SCL	arch od					
SMBUS_SMC_3_SDA	BI	K8	I2C3SDA	arch od					
NEW SMBUS_SMC_4_G3_SCL	BI	N7	I2C4SCL	arch od					
NEW SMBUS_SMC_4_G3_SDA	BI	M7	I2C4SDA	arch od					
NEW SMBUS_SMC_5_S0_SCL	BI	N4	I2C5SCL	arch od					
NEW SMBUS_SMC_5_S0_SDA	BI	N3	I2C5SDA	arch od					
SMC_FAN_0_CTL	OUT	H11	PM6/FAN0PWM0	arch	CPU_PROCHOT_L	IN	K2	C0-	arch analog
SMC_FAN_0_TACH	IN	L13	PM7/FAN0TACH0	arch	SMC_VCCIO_CPU_DIV2	IN	K1	C0+	arch analog
SMC_FAN_1_CTL	OUT	C11	PK6/FAN0PWM1	arch	SMC_PC4	IN	L2	C1-	arch analog
SMC_FAN_1_TACH	IN	A12	PK7/FAN0TACH1	arch	SPI_DESCRIPTOR_OVERRIDE_L	OUT	L1	PC5/C1+	arch
SMC_TOPBLK_SWP_L	OUT	G3	PN2/FAN0PWM2	arch	SMC_CPU_CATERR_L	IN	C5	T3CCP1/PJ5/C2-	arch
TCON_OK SMC_PN3	IN	D10	PN3/FAN0TACH2	proj	CPU_THRMTRIP_3V3	IN	D5	T3CCP0/PJ4/C2+	arch analog
GFX_SMC_ALERT_R	IN	L11	PN4/FAN0PWM3	proj	SMC_PM_G2_EN	OUT	M2	SSI0CLK/PA2	arch
SMC_PN5	OUT	N12	PN5/FAN0TACH3	proj	PM_DSW_PWRGD	OUT	M3	SSI0FSS/PA3	arch
SMC_PN6	OUT	N11	PN6/FAN0PWM4	arch	SMC_DELAYED_PWRGD	OUT	L4	SSI0RX/PA4	arch
LINK_OK SMC_PN7	IN	M11	PN7/FAN0TACH4	proj	SMC_PROCHOT	OUT	N1	SSI0TX/PA5	arch
SMC_PH2	IN	J4	PH2/FAN0PWM5	proj	SMC_DEBUGPRT_RX_L	IN	F11	U1RX/B0	arch
SMC_PH3	OUT	J2	PH3/FAN0TACH5	proj	SMC_DEBUGPRT_TX_L	OUT	E11	U1TX/PB1	arch
CPU_PECI	IN	C4	PECI0RX	arch analog	SMC_PB6	OUT	F4	T0CCP0/PB6	arch pwm
SMC_PECI_L	OUT	C6	PECI0TX	arch	SMC_GFX_THROTTLE_L	OUT	F3	T0CCP1/PB7	arch
SMC_PP0	IN	M13	PP0/IRQ116	proj int	SMC_PF0	IN	M9	SSI1RX/PF0	arch
SMC_PP1	IN	L12	PP1/IRQ117	proj int	SMC_PF1	OUT	N9	SSI1TX/PF1	arch
SMC_PME_S4_WAKE_L	IN	M5	PP2/IRQ118	proj int	SMC_PF2	OUT	L10	SSI1CLK/PF2	arch
SMC_PP3	IN	J12	PP3/IRQ119	proj int	SMC_PF3	OUT	K10	SSI1FSS/PF3	arch
SMC_PP4	OUT	J13	PP4/IRQ120	proj int	S5_PWRGD	IN	L9	PF4	arch
SMC_PP5	IN	L5	PP5/IRQ121	proj int	SMC_PM_PCH_SYS_PWROK	IN	K9	PF5	arch
SMC_PP6	IN	D8	PP6/IRQ122	proj int	SMC_DEBUGPRT_EN_L	OUT	K7	WT0CCP0/PG4	arch
SMC_PP7	IN	K6	PP7/IRQ123	proj int	GFX_SMC_CTF_3V3	IN	L7	WT0CCP1/PG5	arch
ENET_ASF_GPIO	OUT	D4	PQ0/IRQ124	arch od	ALL_SYS_PWRGD	IN	K3	WT2CCP0/PH0	arch
10K PU at I2C page SMC_USBC_INT_L	IN	E4	PQ1/IRQ125	arch int	SMC_THRMTRIP	OUT	K4	WT2CCP1/PH1	arch
SMC_BC_ACOK	IN	F5	PQ2/IRQ126	arch int					
SMC_PQ3	IN	N5	PQ3/IRQ127	arch int	PM_PWRBTN_L	OUT	J3	WT3CCP0/PH4	arch od
74 73 46 37 26 12 PM_SLP_S3_L	IN	N6	PQ4/IRQ128	arch int	PM_SYSRST_L	OUT	H4	WT3CCP1/PH5	arch
73 12 PM_SLP_S4_L	IN	K5	PQ5/IRQ129	arch int	MEM_EVENT_L	OUT	H3	WT4CCP0/PH6	arch od
73 33 12 PM_SLP_S5_L	IN	M6	PQ6/IRQ130	arch int	SMC_PH7	IN	G4	WT4CCP1/PH7	proj
SMC_ONOFF_L	IN	L6	PQ7/IRQ131	arch int					
(to ACE) 46 28 SMC_RX_L (SMC_DEBUGPRT2_RX_L, PA0)	IN	L3	U0RX	arch	SMC_OOB1_D2R_L	IN	C9	T1CCP0/PJ0	
(to ACE) 46 28 SMC_TX_L (SMC_DEBUGPRT2_TX_L, PA1)	OUT	M1	U0TX	arch	SMC_OOB1_R2D_L	OUT	B9	T1CCP1/PJ1	arch
					SMC_PJ2	IN	A9	T2CCP0/PJ2	proj
					SMC_PJ3	OUT	C8	T2CCP1/PJ3	proj
46 SMC_PL7 (SMC_BT_PWR_EN)	BI	E13	USB0DM	proj					
46 SMC_WIFI_PWR_EN (PL6)	BI	E12	USB0DP	arch	SMC_PM3	OUT	H10	WT5CCP1/PM3	arch

(MEM_OK)
(to USB-A Mojo)
(to USB-A Mojo)
(new, Ext_Video_Sel)
GPU's GPIO-19 = CTF
Throttle DIMM
GFX_OK
NEW PCC_ALERT



BOM_COST_GROUP=SMC

PAGE TITLE
SMC: Controller

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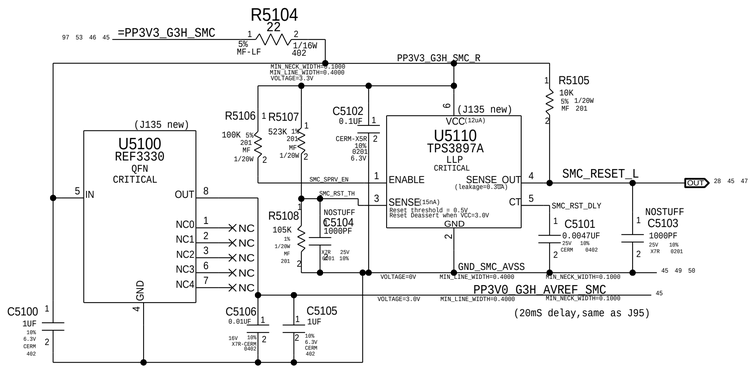
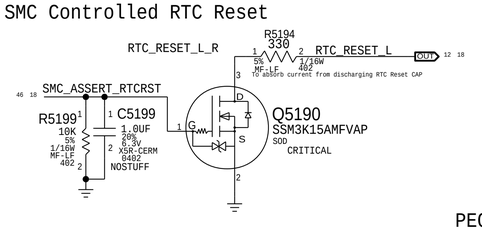
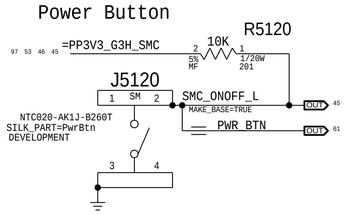
SMC Supervisor and AVREF Supply



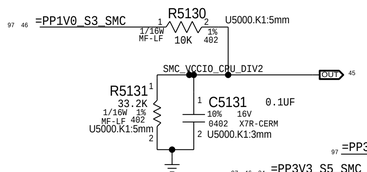
SMC Controlled RTC Reset



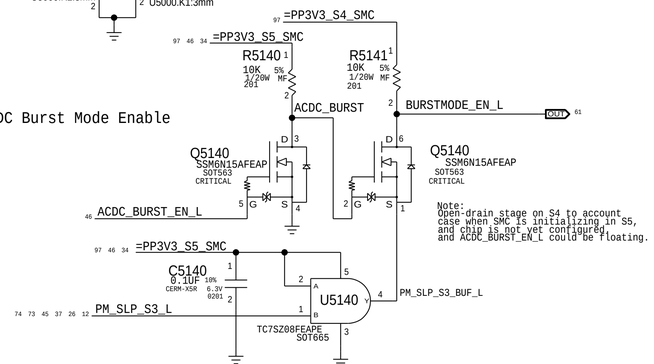
Power Button



Comparator VRef

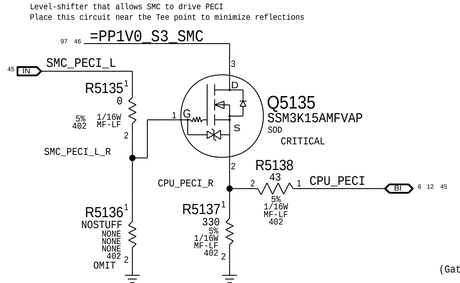


AC/DC Burst Mode Enable



PECI Support

Level-shifter that allows SMC to drive PECI
Place this circuit near the Tee point to minimize reflections



ADC Channel Aliases

SMC_ADC0	VSNS_P12VG3H	MAKE_BASE=TRUE	VD2R
SMC_ADC1	ISNS_P12VG3H	MAKE_BASE=TRUE	ID2R
SMC_ADC2	ISNS_P5V_S4	MAKE_BASE=TRUE	IR54
SMC_ADC3	ISNS_P12VS0_CPUCORE	MAKE_BASE=TRUE	ID20
SMC_ADC4	VSNS_CPUVCC	MAKE_BASE=TRUE	VC0C
SMC_ADC5	ISNS_CPUVCC	MAKE_BASE=TRUE	IC0C
SMC_ADC6	VSNS_CPUVCC_GT	MAKE_BASE=TRUE	VC0G
SMC_ADC7	ISNS_CPUVCC_GT	MAKE_BASE=TRUE	IC0G
SMC_ADC8	ISNS_CPUVCC_IO	MAKE_BASE=TRUE	IC0I
SMC_ADC9	ISNS_P1V2S0	MAKE_BASE=TRUE	IC0M
SMC_ADC10	ISNS_CPUVCC_SA	MAKE_BASE=TRUE	IC0S
SMC_ADC11	ISNS_P12VS0_FBVDDQ	MAKE_BASE=TRUE	IG1F
SMC_ADC12	VSNS_GPUCORE_ALT	MAKE_BASE=TRUE	VG0C
SMC_ADC13	ISNS_GPUCORE_ALT	MAKE_BASE=TRUE	IG0C
SMC_ADC14	VSNS_GPU_VDDCI	MAKE_BASE=TRUE	VG0I
SMC_ADC15	ISNS_GPU_VDDCI	MAKE_BASE=TRUE	IG0I
SMC_ADC16	ISNS_P12VS0_GPU_AUX	MAKE_BASE=TRUE	IG1A
SMC_ADC17	ISNS_P12VS0_GPUCORE	MAKE_BASE=TRUE	IG1C
SMC_ADC18	ISNS_P12VS0_HDD	MAKE_BASE=TRUE	IH02
SMC_ADC19	ISNS_HDDS0	MAKE_BASE=TRUE	IH05
SMC_ADC20	ISNS_P3V3_S5	MAKE_BASE=TRUE	IR35
SMC_ADC21	ISNS_SSD_S4	MAKE_BASE=TRUE	IH1R
SMC_ADC22	VSNS_VDDQS3_DDR	MAKE_BASE=TRUE	VM0R
SMC_ADC23	ISNS_VDDQS3_DDR	MAKE_BASE=TRUE	IM0R

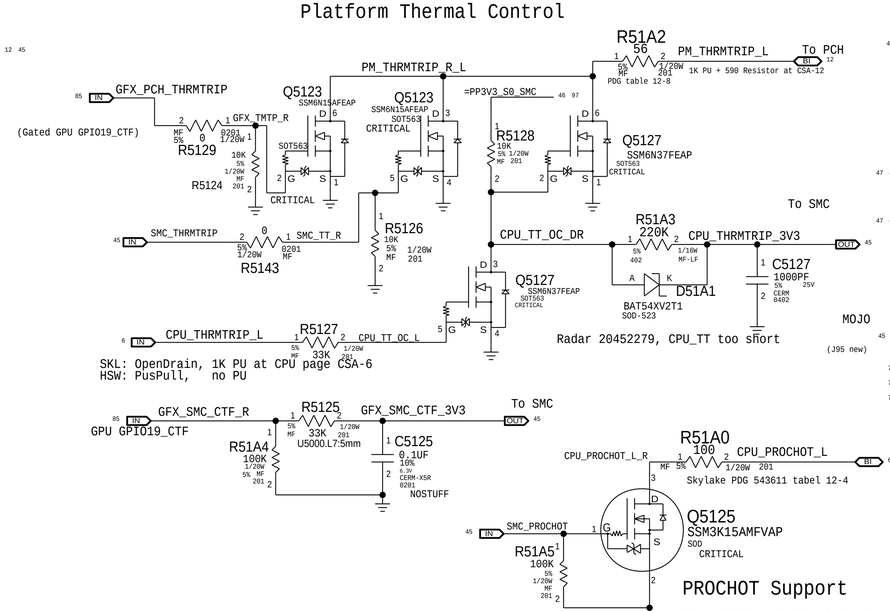
Project-specific Aliases

SMC_PN5	ACDC_BURST_EN_L	MAKE_BASE=TRUE		
SMC_PJ3	SMC_OOB2_R2D_L	MAKE_BASE=TRUE		
SMC_PJ2	SMC_OOB2_D2R_L	MAKE_BASE=TRUE		
SMC_PP0	SMC_ACDC_ID	MAKE_BASE=TRUE		
SMC_PH2	SMC_ASSERT_RTCRST	MAKE_BASE=TRUE		
SMC_PL7	SMC_BT_PWR_EN	MAKE_BASE=TRUE		
SMC_PC4	MEM_OK	MAKE_BASE=TRUE	(NEW, LED-7)	(100K PD AT PCH)
SMC_PH7	GFX_OK	MAKE_BASE=TRUE	(LED-3)	(10K PD AT GPU)
SMC_PN7	DP_LINK_OK	MAKE_BASE=TRUE	(LED-3)	(10K PD AT GPU)
SMC_PN3	TCON_BLC_EN	MAKE_BASE=TRUE	(LED-4)	(100K PD AT BLC)
SMC_PM3	PSU_OCP_ACTIVE	MAKE_BASE=TRUE	(NEW)	
SMC_PP1	PM_EPO_SMC_L	MAKE_BASE=TRUE	(NEW)	
SMC_PH3	SMC_HI_PWR_GFX	MAKE_BASE=TRUE	(NEW)	
SMC_PB6	SMC_EXT_VIDEO_SEL	MAKE_BASE=TRUE	(NEW)	

Unused Project-specific

SMC_PF0	NC_SMC_PF0	MAKE_BASE=TRUE	
SMC_PF1	NC_SMC_PF1	MAKE_BASE=TRUE	
SMC_PF2	NC_SMC_PF2	MAKE_BASE=TRUE	NO_TEST=1
SMC_PF3	NC_SMC_PF3	MAKE_BASE=TRUE	NO_TEST=1
SMC_PN6	NC_SMC_PN6	MAKE_BASE=TRUE	NO_TEST=1
SMC_PP3	NC_SMC_PME_S4_DARK_L	MAKE_BASE=TRUE	NO_TEST=1
SMC_PP4	NC_SMC_S4_WAKESRC_EN	MAKE_BASE=TRUE	
SMC_PP5	NC_SMC_PP5	MAKE_BASE=TRUE	NO_TEST=1
SMC_PP6	NC_SMC_PP6	MAKE_BASE=TRUE	NO_TEST=1
SMC_PP7	NC_SMC_PP7	MAKE_BASE=TRUE	NO_TEST=1
SMC_PQ3	PM_SLP_S0_L	MAKE_BASE=TRUE	
SMC_OOB1_R2D_L	NC_SMC_OOB1_R2D_L	MAKE_BASE=TRUE	NO_TEST=1
SMC_PH3	NC_SMC_PH3	MAKE_BASE=TRUE	NO_TEST=1

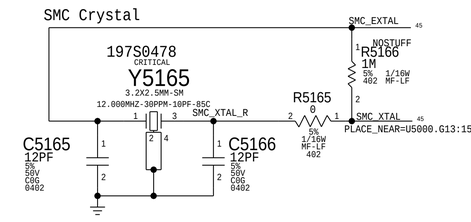
Platform Thermal Control



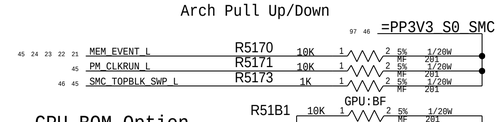
PROCHOT Support

BOM_COST_GROUP=SMC

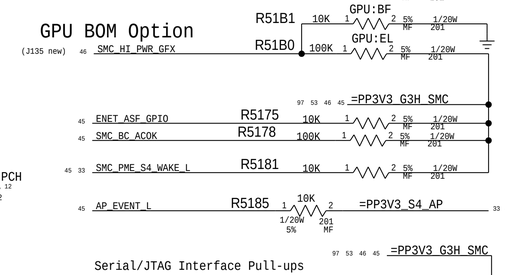
SMC Crystal



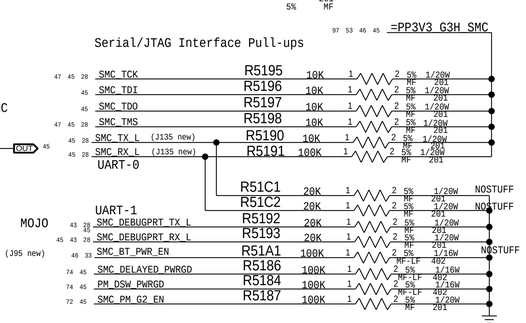
Arch Pull Up/Down



GPU BOM Option



Serial/JTAG Interface Pull-ups



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SMC: Controller Support

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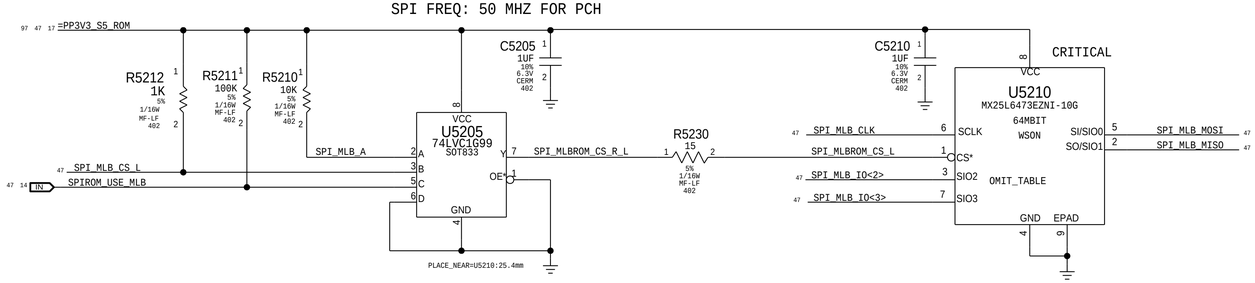
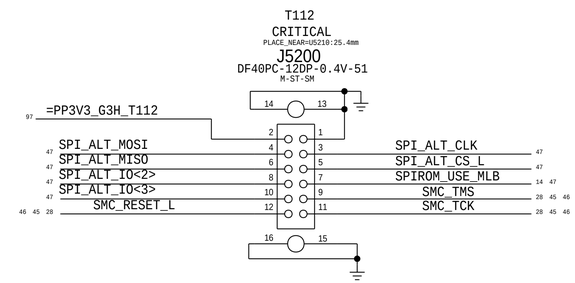
SPI BootROM

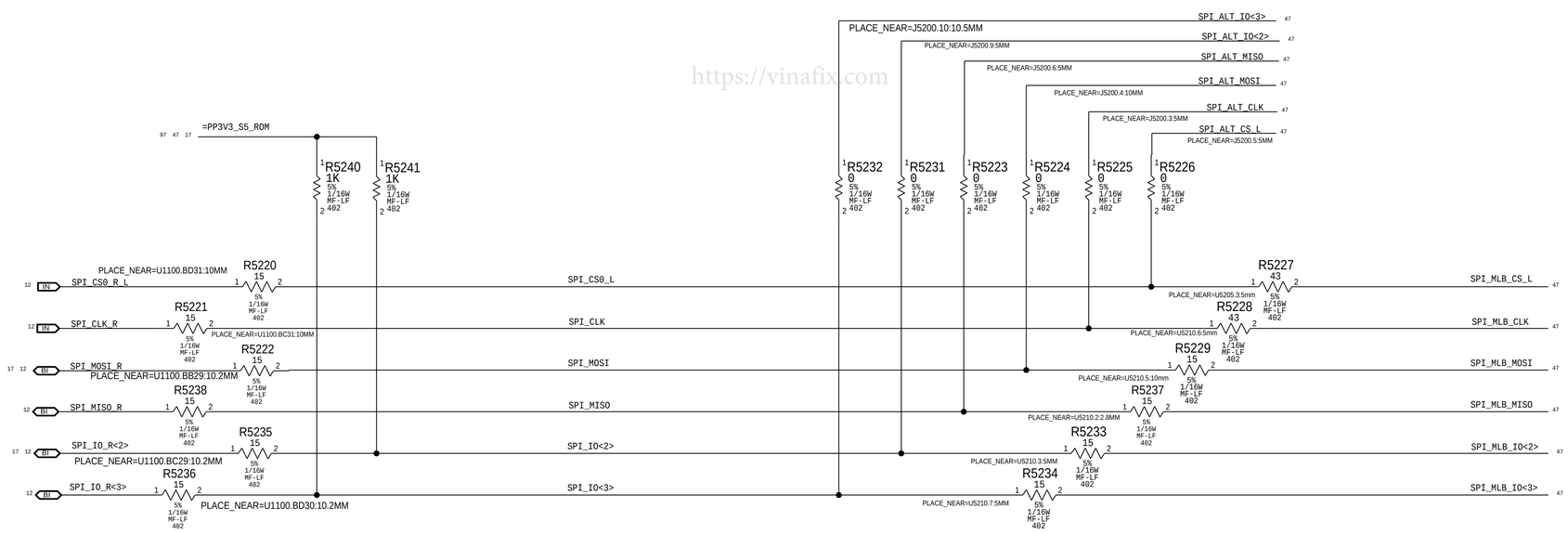
QUAD_IO MODE (MODE 0 & 3) SUPPORTED
SPI FREQ: 50 MHZ FOR PCH



T112 Connector



SPI Series Termination



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BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=ANDREW SYNC_DATE=02/23/2010

PAGE TITLE
CPU & CHIPSET: SPI and Debug Connector

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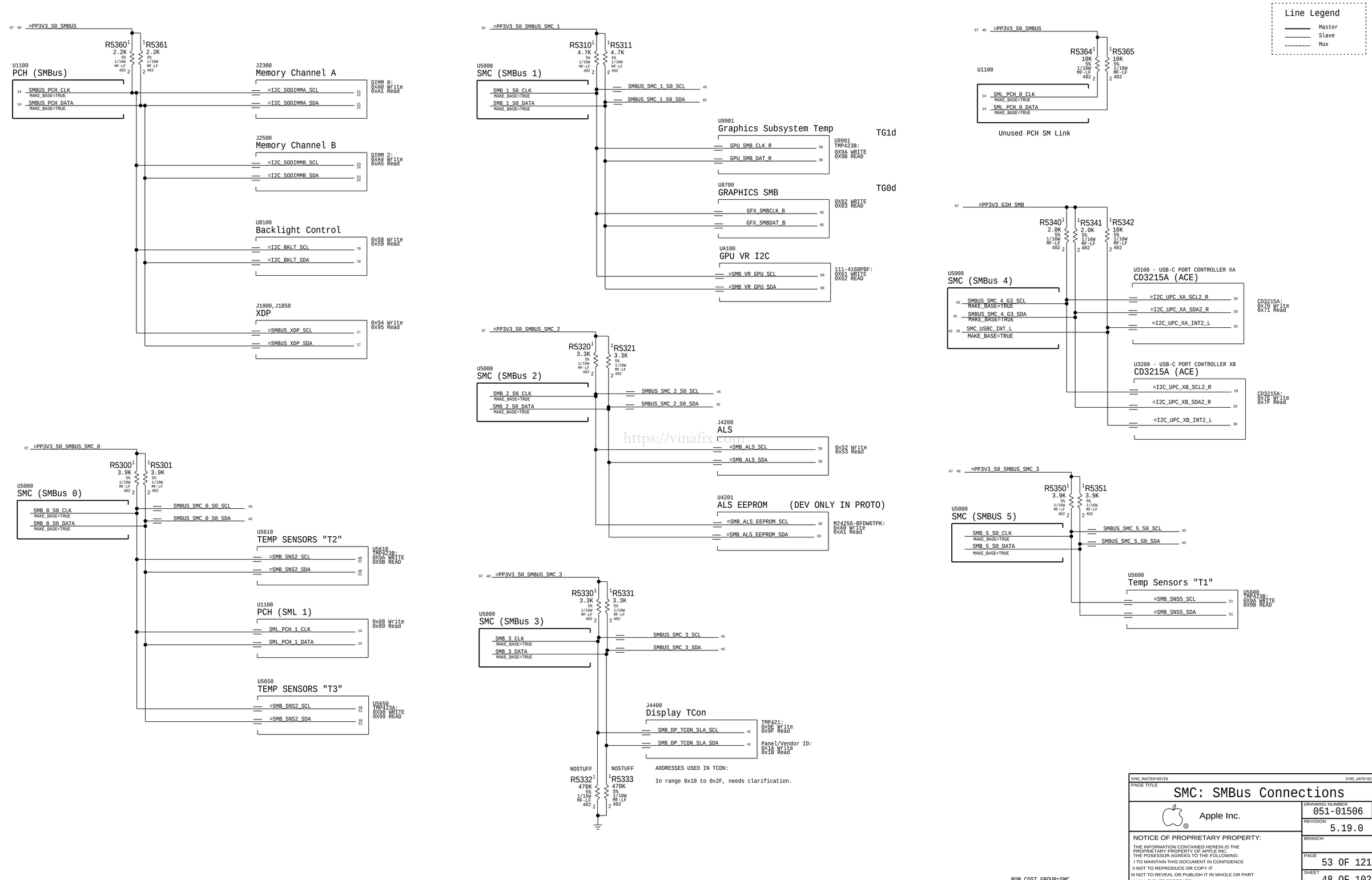

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SYNC_MASTER=KEVIN SYNC_DATE=02/04/2016

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SMC: SMBus Connections

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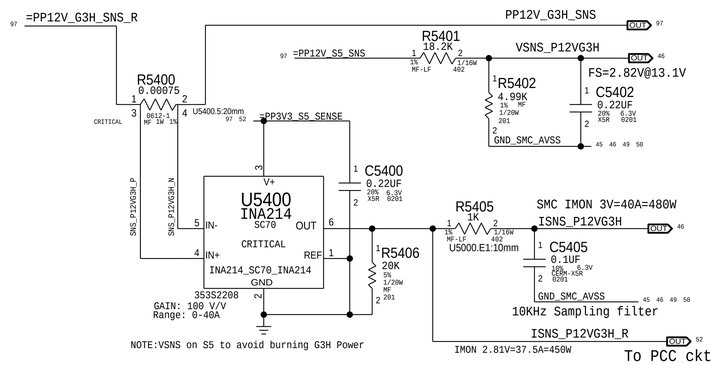
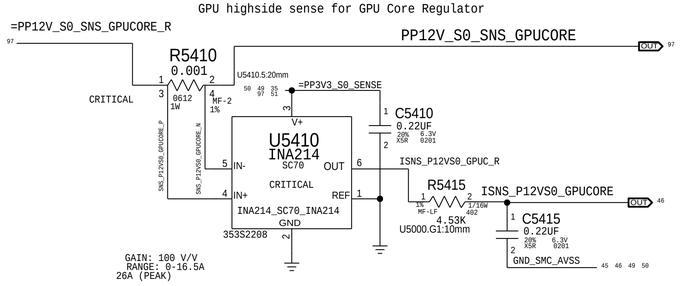
12V G3H (VD2R:ADC0/ID2R:ADC1)

AC/DC lowside sense (System total)



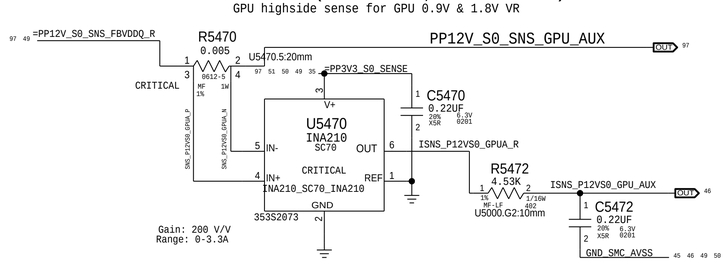
PP12V_S0_GPU (VG1C=VD20, IG1C:ADC17)

GPU highside sense for GPU Core Regulator



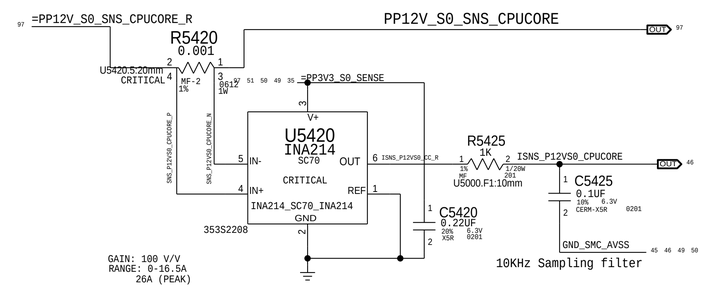
GPU AUX RAILS (VG1A=VD20, IG1A:ADC16)

GPU highside sense for GPU 0.9V & 1.8V VR



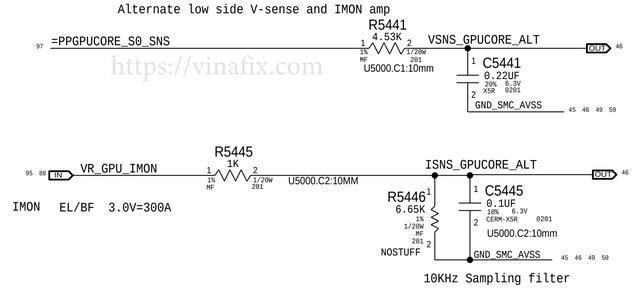
PP12V_S0_CPU (VD20:ADC2 /ID20:ADC3)

CPU highside sense for CPU Core Regulator



GPU Core - Alt (VG0C:ADC12/IG0C:ADC13)

Alternate low side V-sense and IMON amp



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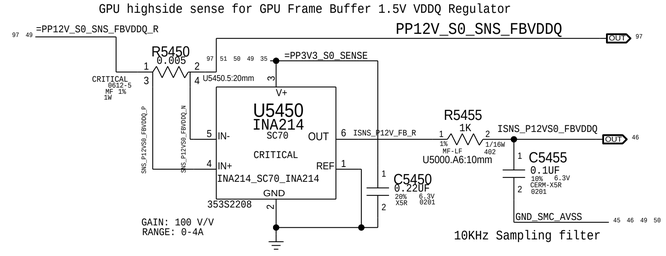
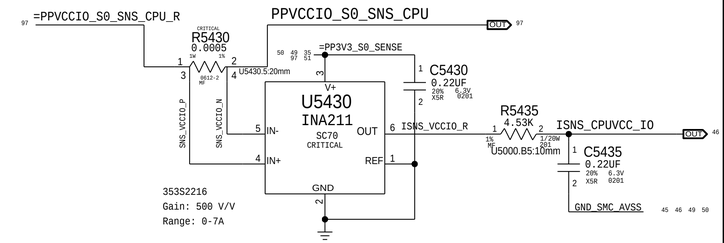
GPU FB (VG1F=VD20, IG1F:ADC11)

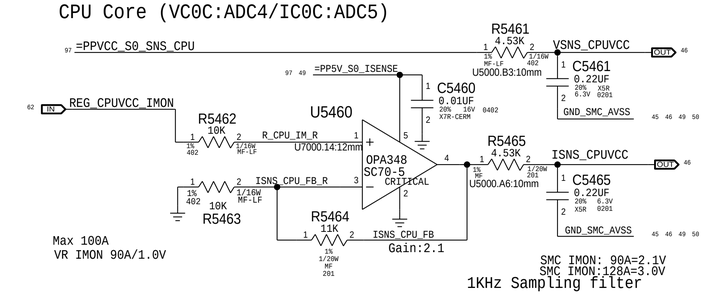
GPU highside sense for GPU Frame Buffer 1.5V VDDQ Regulator



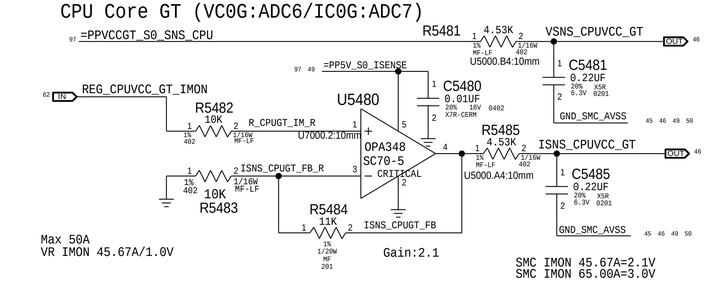
CPU VCCIO (VC0I=0.95V, IC0I:ADC8)



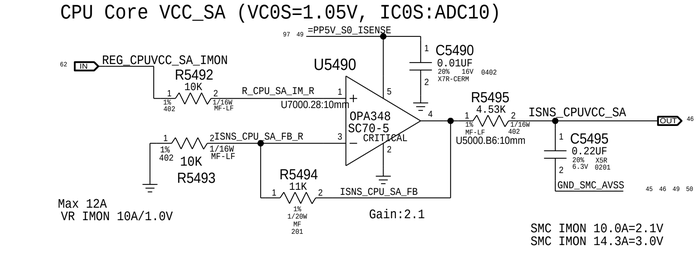
CPU Core (VC0C:ADC4/IC0C:ADC5)



CPU Core GT (VC0G:ADC6/IC0G:ADC7)



CPU Core VCC_SA (VC0S=1.05V, IC0S:ADC10)



BOM_COST_GROUP=Sensors

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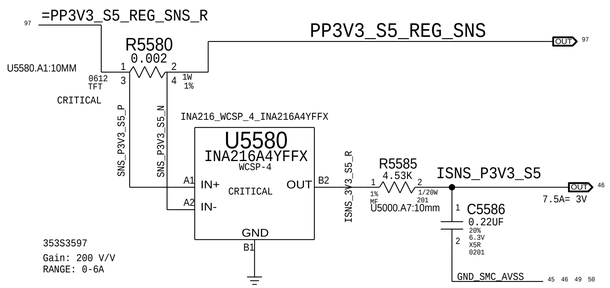
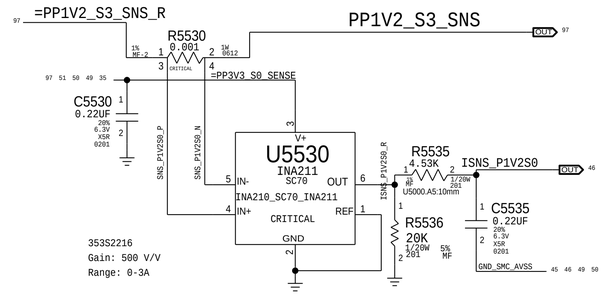
3V3_S5 (VC0M=3.3, IC35:ADC20)

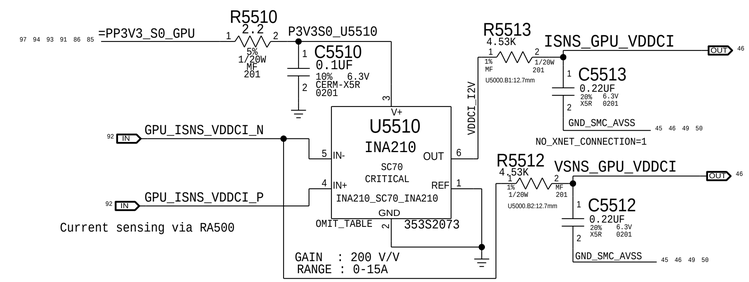


VDDQ S3 (VC0M=VM0R, IC0M:ADC9)

VDDQ lowside sense for SO-DIMM modules



GPU_VDDCI S0 (VG0I:ADC14 /IG0I: ADC15)

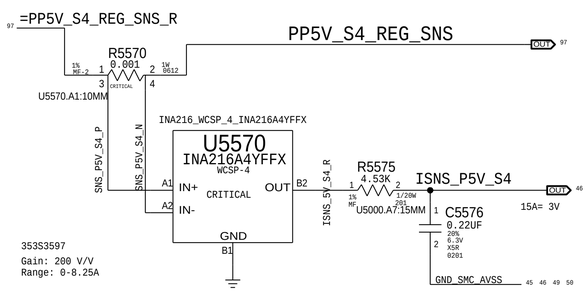


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S2073	1	IC,INA210, 200V/V SC70-6	U5510	GPU:EL
353S2208	1	IC,INA214, 100V/V SC70-6	U5510	GPU:BF

RA500 = 0.5_mOHM

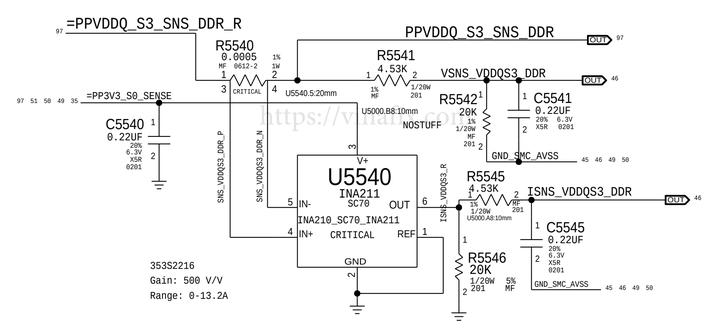
RA500 = 1.0_mOHM

5V_S4 (VC0M=5.0, IC54:ADC2)



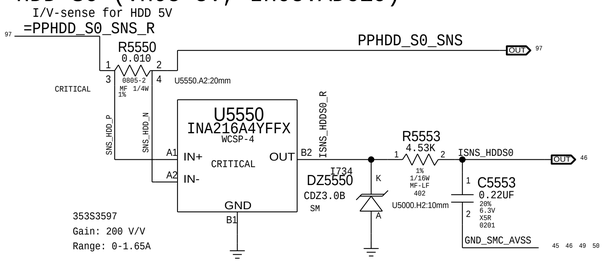
VDDQ S3 (VM0R:ADC22/ IM0R:ADC23)

VDDQ lowside sense for SO-DIMM modules



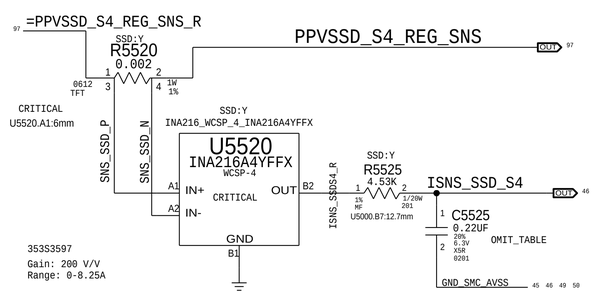
HDD S0 (VH05=5V, IH05:ADC19)

I/V-sense for HDD 5V



SSD S0 (VR1R:ADC20 / IH1R:ADC21)

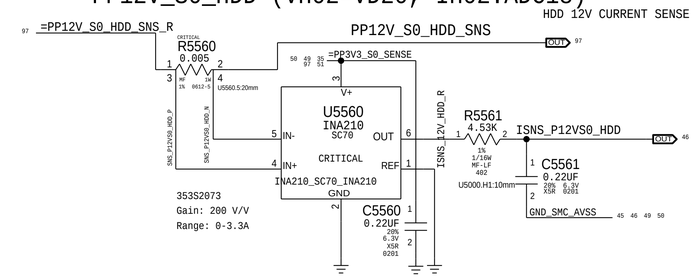
I-SENSE FOR SSD / V-SENSE FOR PPSSD_S4)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0304	1	CAP,0.22UF,201	C5525	SSD:Y
117S0201	1	RES,0 OHM,201	C5525	SSD:N

PP12V_S0_HDD (VH02=VD20, IH02:ADC18)

HDD 12V CURRENT SENSE



BOM_COST_GROUP=Sensors

PAGE TITLE

SENSORS: I and V Sense(Continued)

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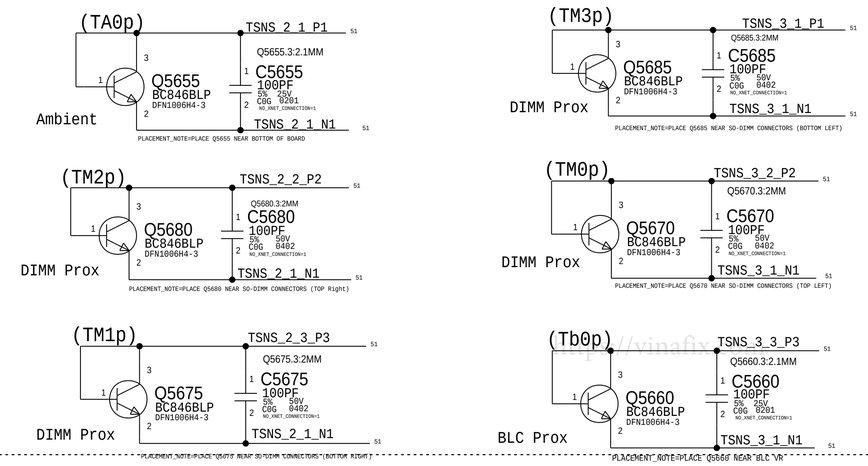

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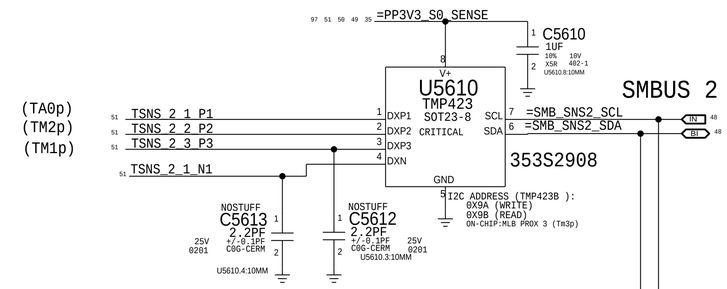
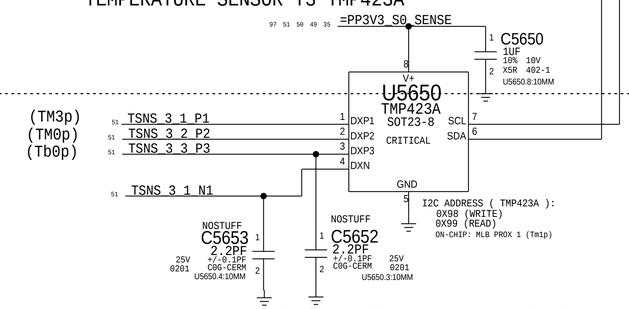
TEMPERATURE SENSOR T2 TMP423B

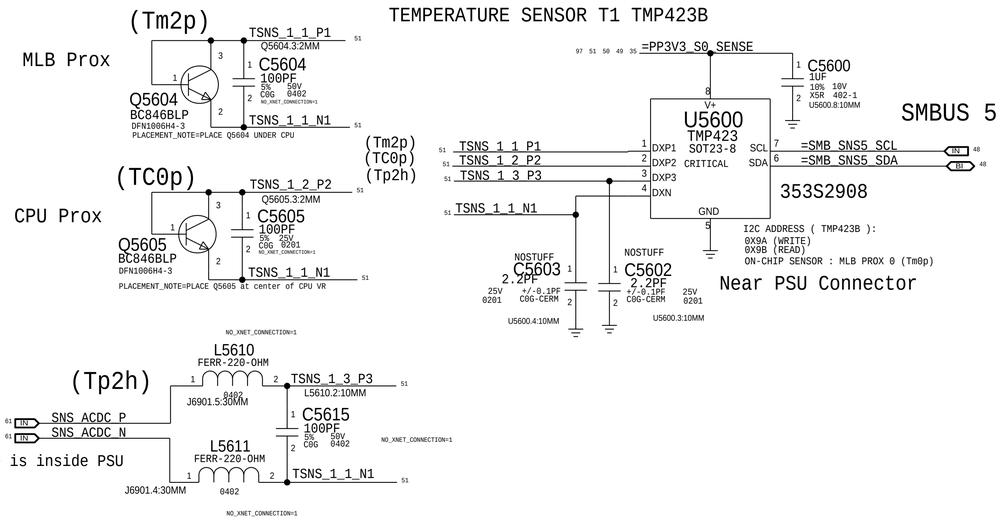


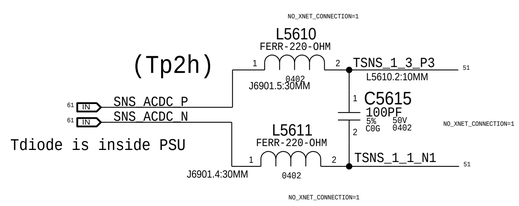
TEMPERATURE SENSOR T3 TMP423A



Below GPU,next to SMC

TEMPERATURE SENSOR T1 TMP423B





BOM_COST_GROUP=Sensors

PAGE TITLE	SENSORS: Temperature Sensors
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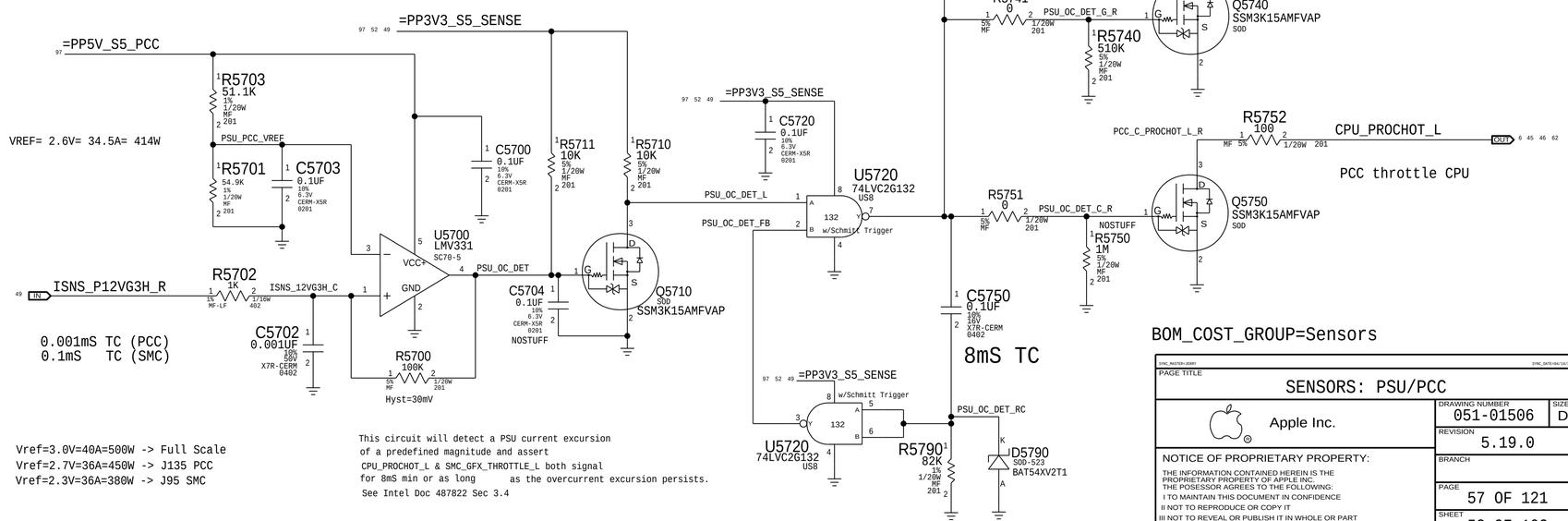
Fast Response PSU Overcurrent Protection



Vref=3.0V=40A=500W -> Full Scale
Vref=2.7V=36A=450W -> J135 PCC
Vref=2.3V=36A=380W -> J95 SMC

This circuit will detect a PSU current excursion
of a predefined magnitude and assert
CPU_PROCHOT_L & SMC_GFX_THROTTLE_L both signal
for 8mS min or as long as the overcurrent excursion persists.
See Intel Doc 487822 Sec 3.4

BOM_COST_GROUP=Sensors

SYNC_MASTER=JERRY SYNC_DATE=06/14/2018

PAGE TITLE

SENSORS: PSU/PCC

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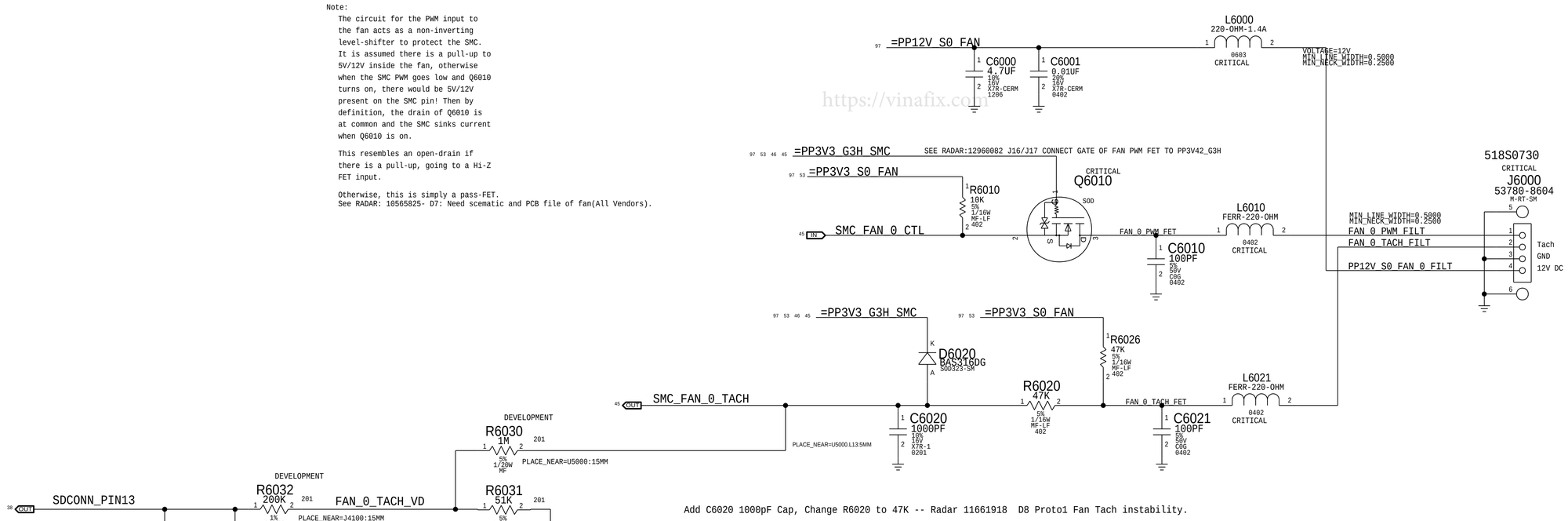
SMC Fan 0 (System)

Note:
The circuit for the PWM input to the fan acts as a non-inverting level-shifter to protect the SMC. It is assumed there is a pull-up to 5V/12V inside the fan, otherwise when the SMC PWM goes low and Q6010 turns on, there would be 5V/12V present on the SMC pin! Then by definition, the drain of Q6010 is at common and the SMC sinks current when Q6010 is on.

This resembles an open-drain if there is a pull-up, going to a Hi-Z FET input.

Otherwise, this is simply a pass-FET.
See RADAR: 10565825- D7: Need scematic and PCB file of fan(All Vendors).



Add C6020 1000pF Cap, Change R6020 to 47K -- Radar 11661918 D8 Proto1 Fan Tach instability.

SMC Fan 1 (Unused)

45 IN SMC_FAN_1_CTL — NC_SMC_FAN_1_CTL
MAKE_BASE=TRUE NO_TEST=1

45 OUT SMC_FAN_1_TACH — NC_SMC_FAN_1_TACH
MAKE_BASE=TRUE

BOM_COST_GROUP=FAN

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SYNC_MASTER=ANDREW SYNC_DATE=04/06/2016

PAGE TITLE
FAN: System Fan

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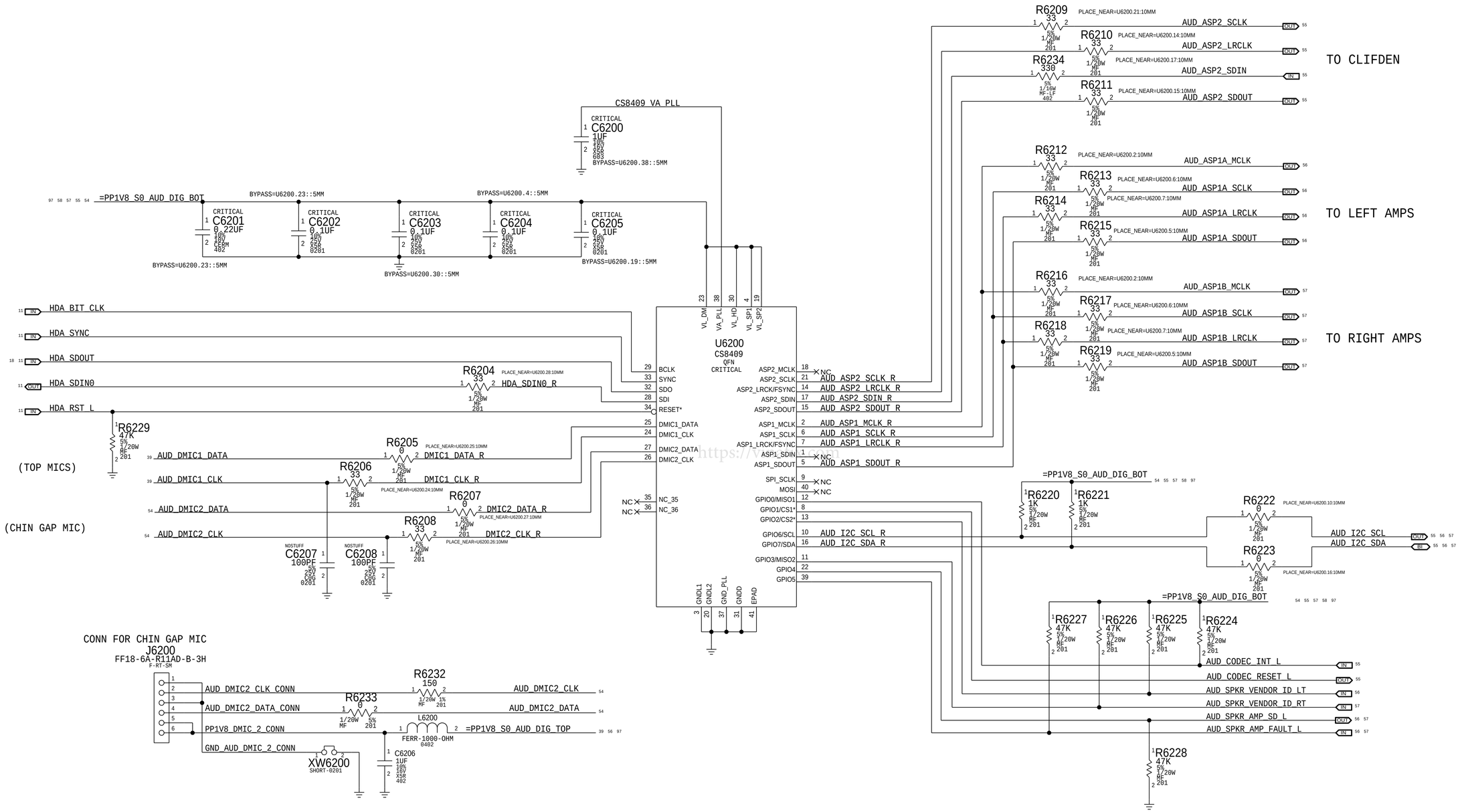

DESIGN: X502/MLB
LAST CHANGE: Tue Aug 18 12:55:20 2015

PAGE TITLE
AUDIO: HDA BRIDGE

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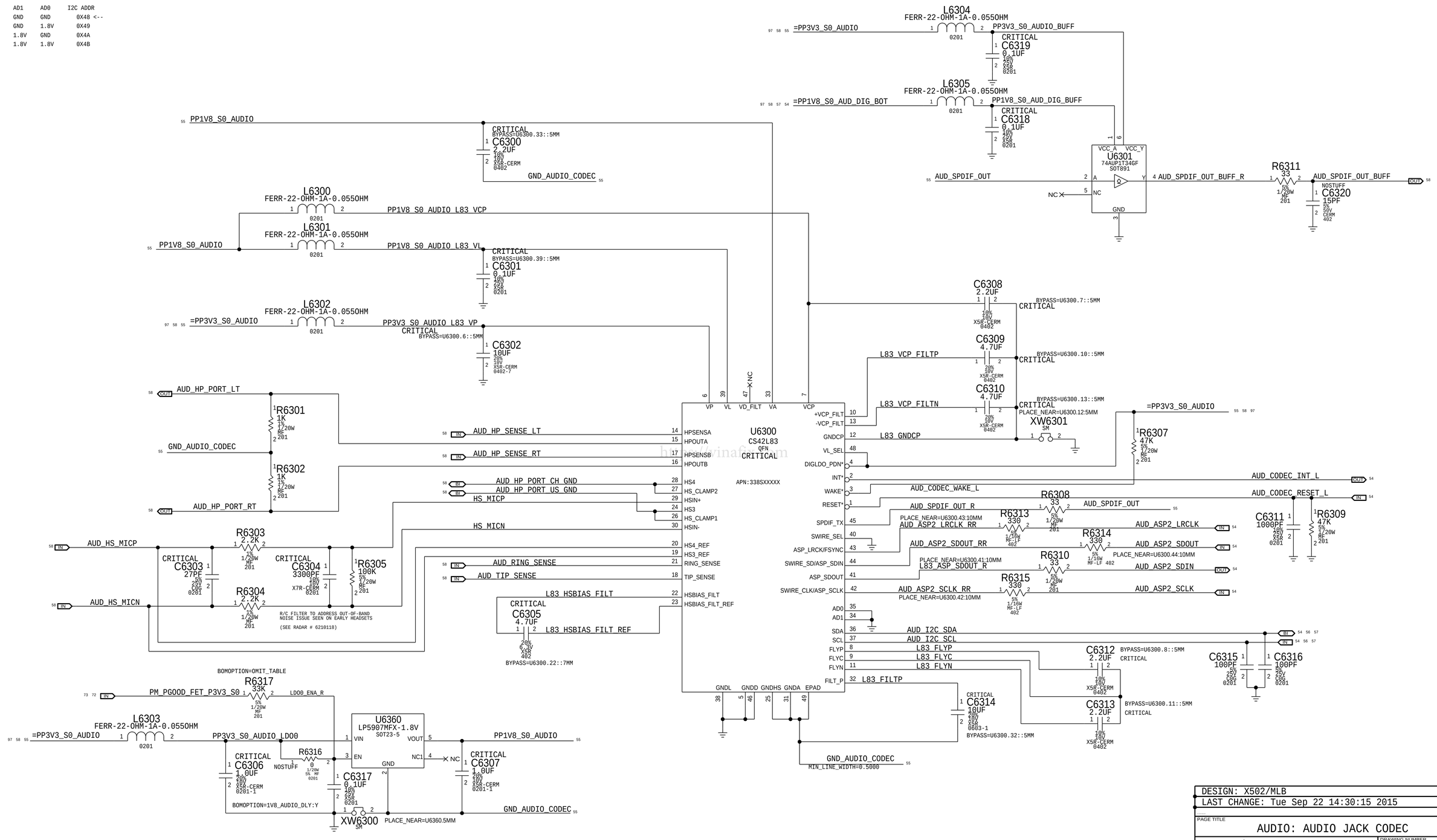
AD1	AD0	I2C ADDR
GND	GND	0X48 <--
GND	1.8V	0X49
1.8V	GND	0X4A
1.8V	1.8V	0X4B



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
117S0083	1	RES,33K,OHM,201	R6317	1V8_AUDIO_DLY:Y	<----- J133/134
117S0201	1	RES,0 OHM,201	R6317	1V8_AUDIO_DLY:N	<----- J135

DESIGN: X502/MLB
LAST CHANGE: Tue Sep 22 14:30:15 2015

PAGE TITLE
AUDIO: AUDIO JACK CODEC

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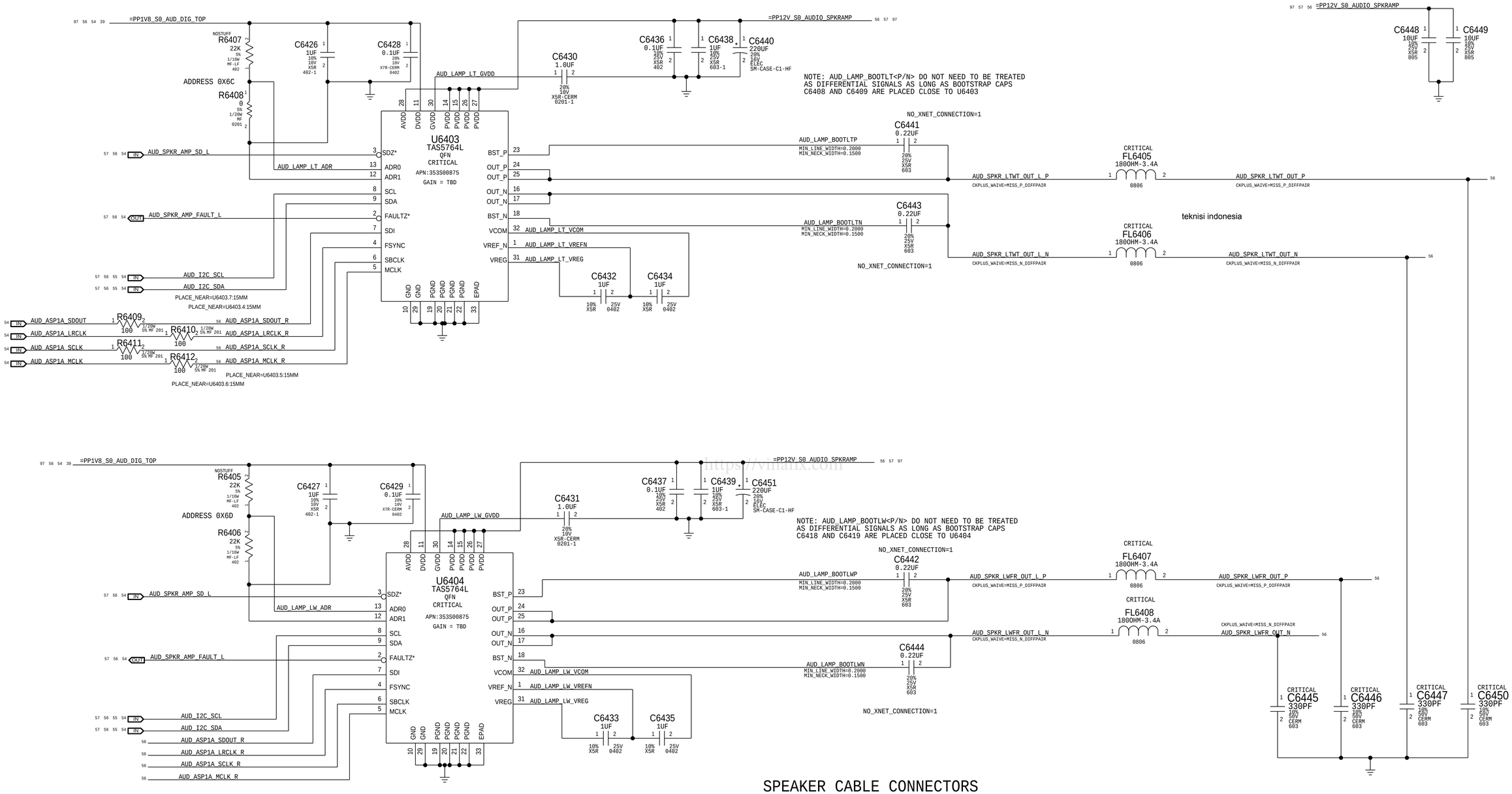
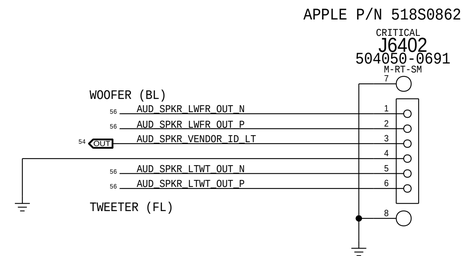
2X MONO SPEAKER AMPLIFIERS (TAS5764L)

SPEAKER AMPLIFIERS - LEFT CHANNEL



SPEAKER CABLE CONNECTORS

APPLE P/N 518S0862



BOM_COST_GROUP=AUDIO

DESIGN: X502/DEV_MLB_U
LAST CHANGE: Wed Feb 18 17:12:24 2015

PAGE TITLE
AUDIO: LEFT SPKR AMP

Apple Inc.

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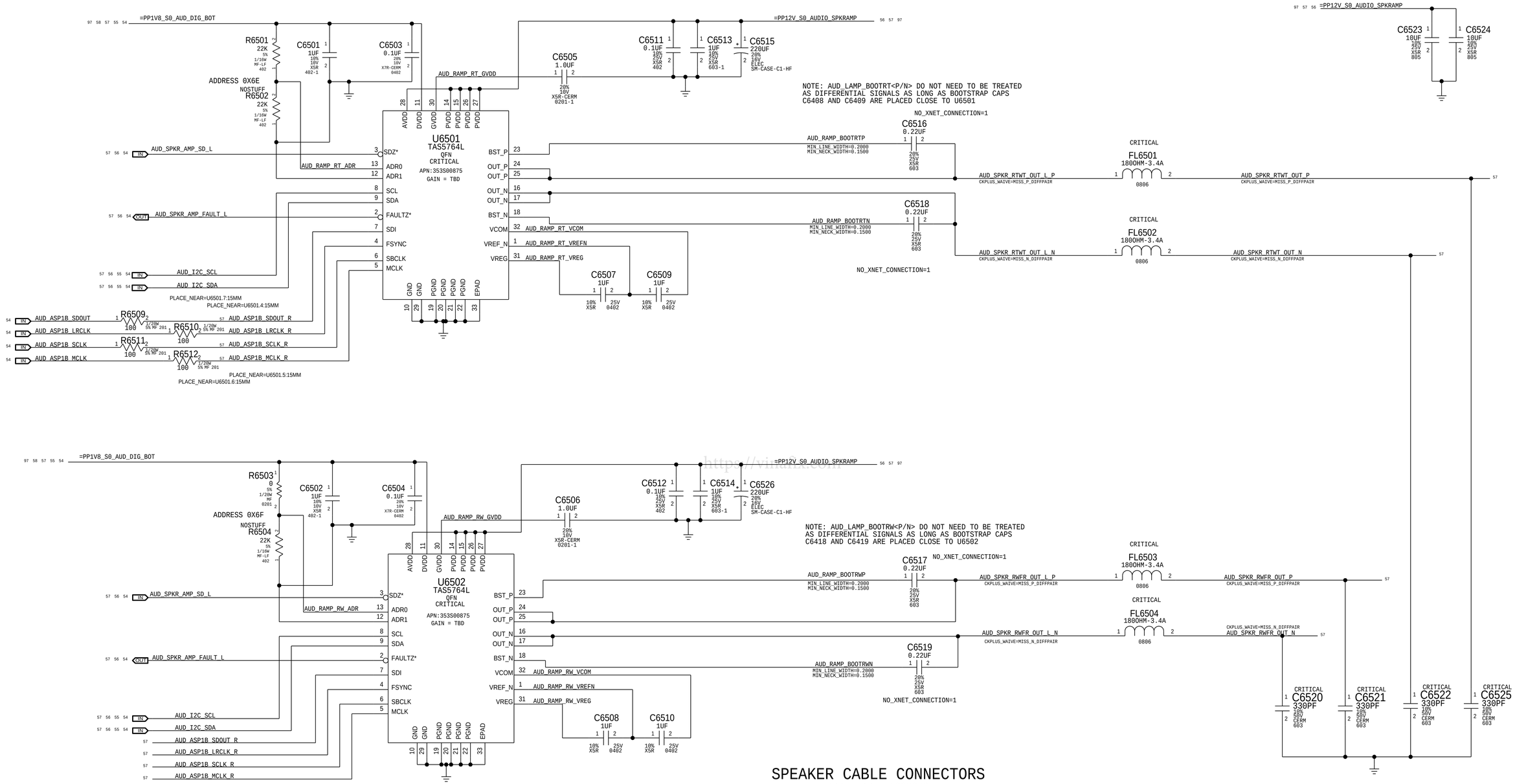
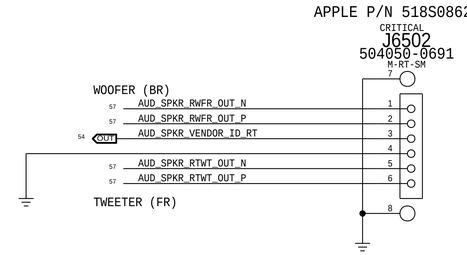
2X MONO SPEAKER AMPLIFIERS (TAS5764L)

SPEAKER AMPLIFIERS - RIGHT CHANNEL



SPEAKER CABLE CONNECTORS

APPLE P/N 518S0862



BOM_COST_GROUP=AUDIO

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LAST CHANGE: Wed Feb 18 17:12:24 2015	
PAGE TITLE: AUDIO: RIGHT SPKR AMP	
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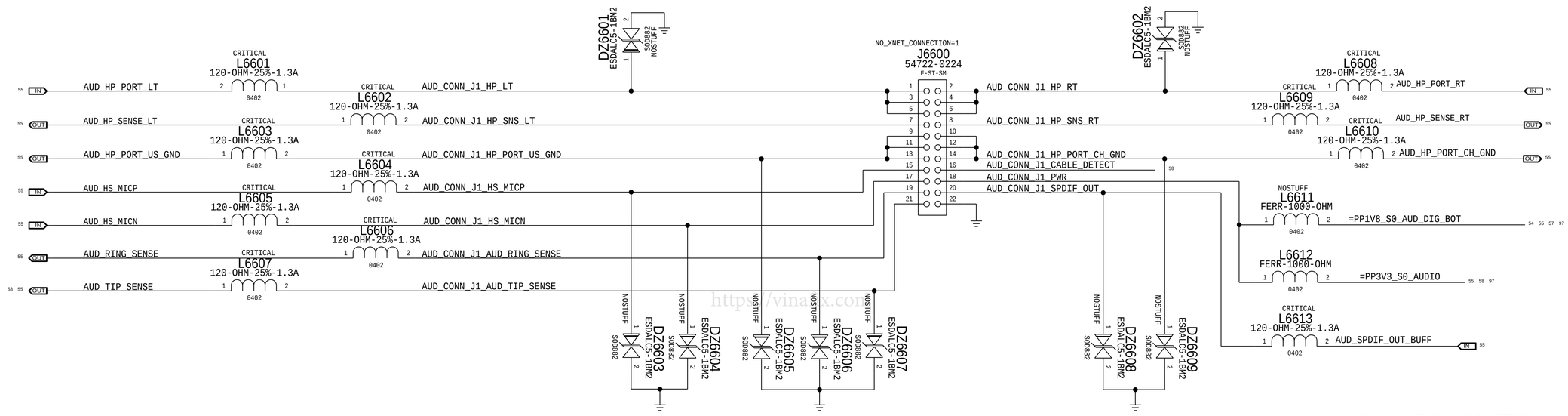
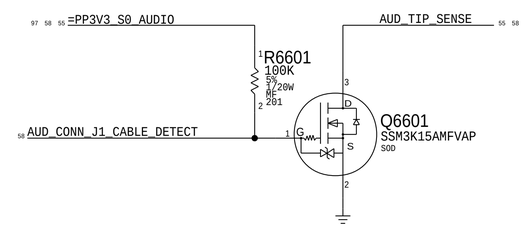


AUDIO JACK FLEX CABLE DETECT



BOM_COST_GROUP=AUDIO

PAGE TITLE	AUDIO: AUDIO JACK CONN
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SYNC_MASTER:JAMES(AUD31) SYNC_DATE:03/28/2019

PAGE TITLE

AUDIO: EMPTY

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	MAC SHDN	WIN SHDN	DET ASSIGNMENT
HP/LINE OUT	0X03 (3)	0X03 (3)	0X0A (10,D)	GPIO_2	GPIO_2	0X0A (DET D)
PRIMARY SPKRS (WFR)	0X04 (4)	0X04 (4)	0X0B (11)	MICBIAS	GPIO_3	N/A
SECONDARY SPKRS (TWT)	0X03 (3)	0X03 (3)	0X0A (10,V24)	MICBIAS	N/A	N/A
SPDIF OUT	N/A	0X08 (8)	0x10 (16)	N/A	N/A	0X0D (DET B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
SPDIF IN	0X07 (7)	0x0F (15)	N/A	0X09 (DET A)
INTERNAL MIC ARRAY	0X06 (6) 0X05 (5)	0X0E (14,LEFT & RIGHT) 0X12 (18,LEFT)	N/A	N/A
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	Lynx POINT GPIO 16	Lynx POINT GPIO 5 (RCVR INT) Lynx POINT GPIO 3 (PERIPH DET)

OTHER DETECT

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
MULTIPLE SPKR VENDORS	N/A	N/A	N/A	0X0C (DET C)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	0.1 MM	?
SPKROUT	*	0.2 MM	?

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
SPKROUTDIFF	*	SPKROUTDIFF

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIODIFF	*	Y	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
SPKROUTDIFF	*	Y	0.6 MM	0.25 MM	10 MM	0.2 MM	0.2 MM

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SYNC_MASTER=JAMES(AUDIO) SYNC_DATE=02/23/2010

PAGE TITLE

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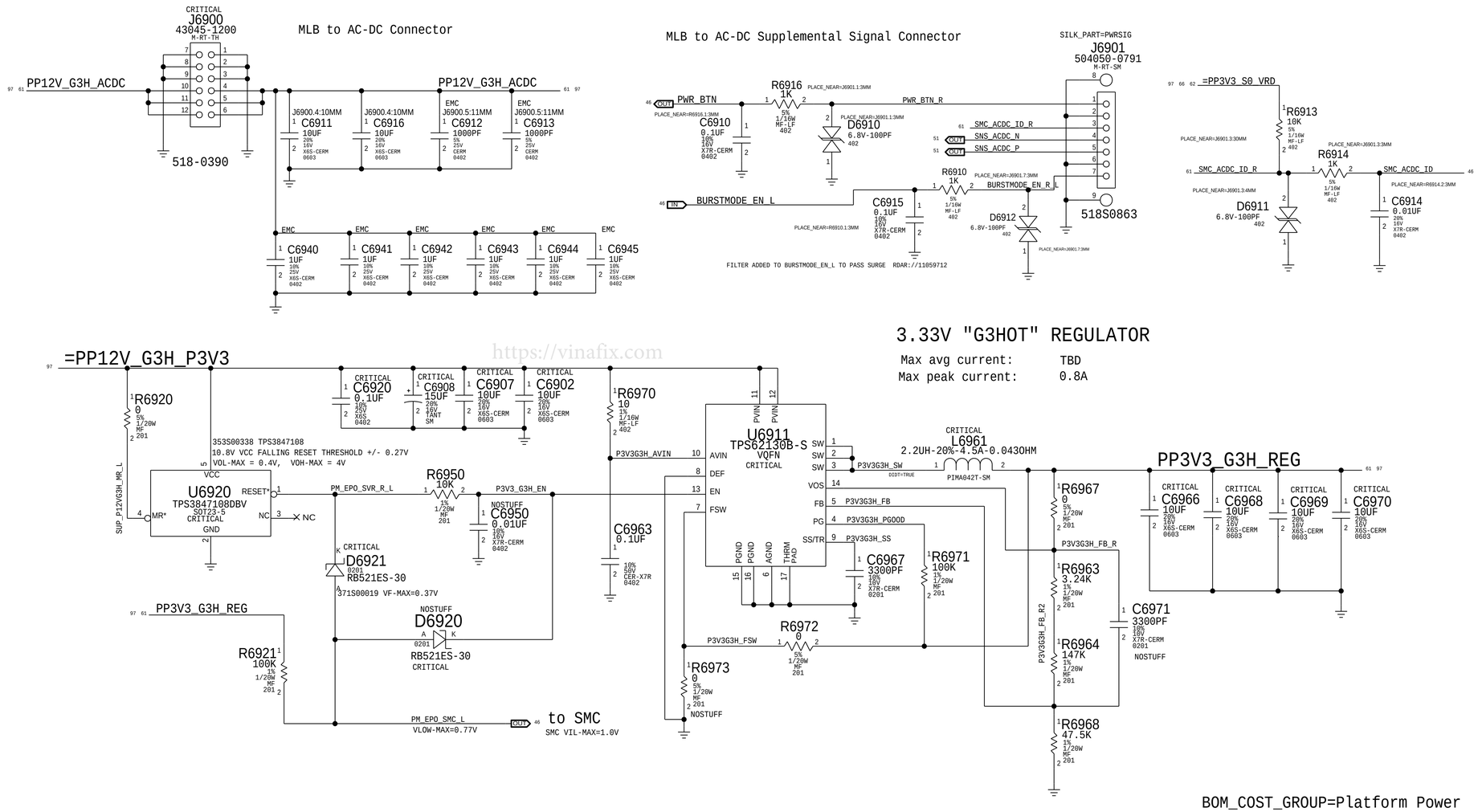

3.33V "G3HOT" REGULATOR

Max avg current: TBD
Max peak current: 0.8A

BOM_COST_GROUP=Platform Power

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teknisi indonesia

PAGE TITLE	PLATFORM POWER: Connectors / VReg G3Hot
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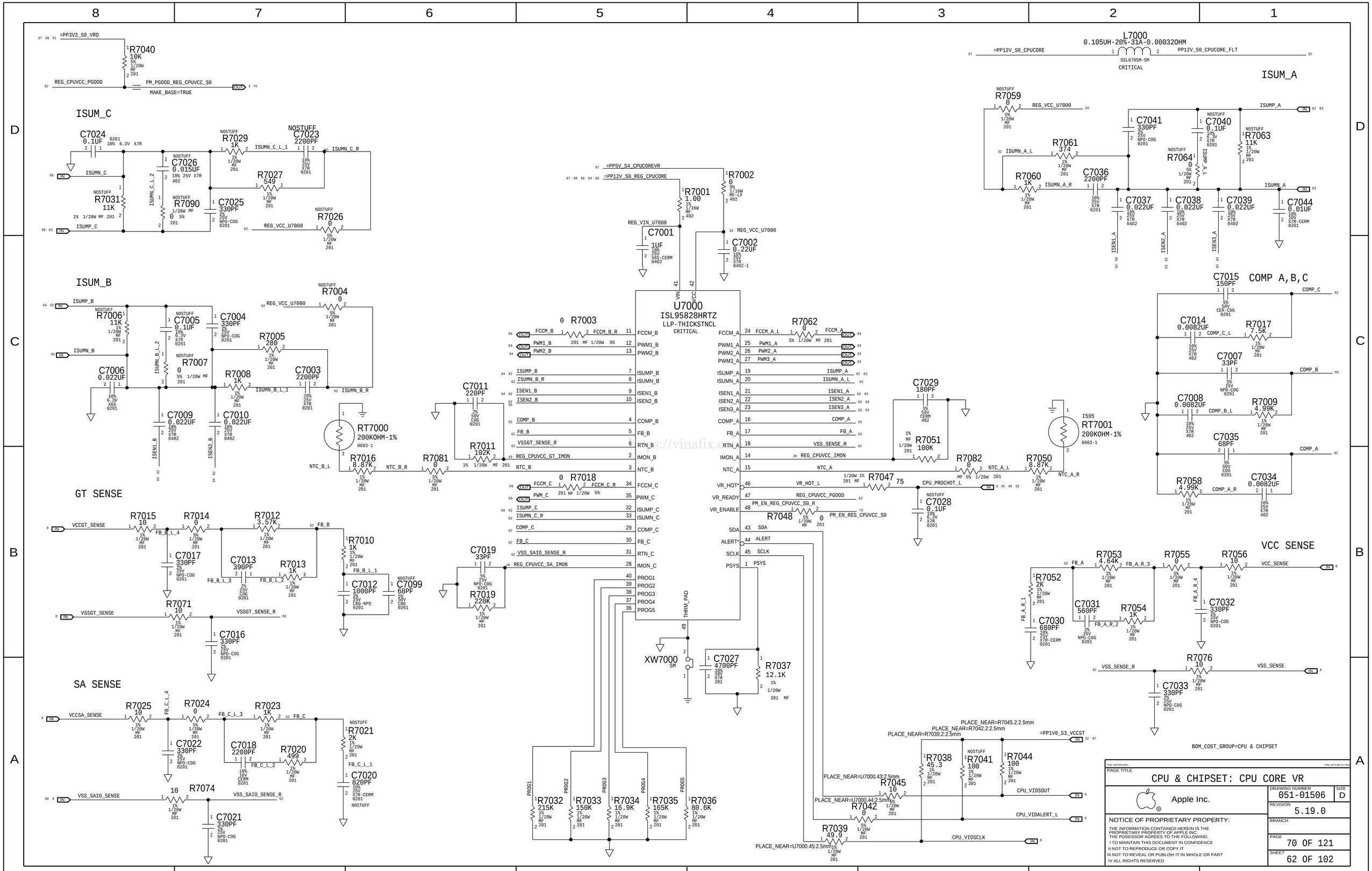
ISUM_C
ISUM_B
GT SENSE
SA SENSE
ISUM_A
COMP A,B,C
VCC SENSE
U7000
ISL95828HRTZ
LLP-THICKSTNCL
CRITICAL
L7000
0.105UH-20%-31A-0.000320HM
SSL0705M-SM
CRITICAL
RT7000
200KOHM-1%
RT7001
200KOHM-1%
XW7000
BOM_COST_GROUP=CPU & CHIPSET
PAGE TITLE
CPU & CHIPSET: CPU CORE VR
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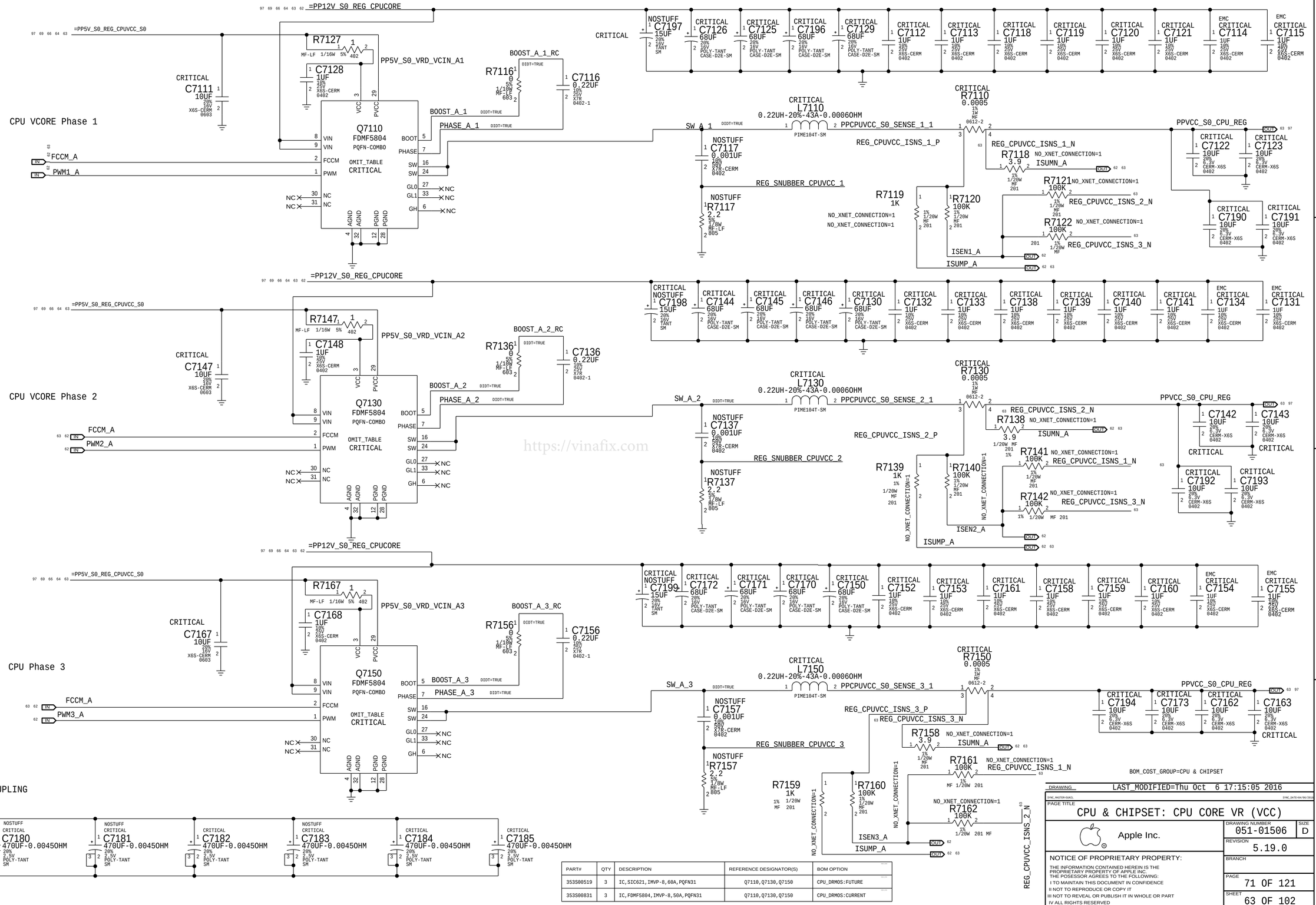
CPU VCC Regulator
EDC = 100A
TDC = 70A



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S00519	3	IC,SIC621,IMVP-8,60A,PQFN31	Q7110,Q7130,Q7150	CPU_DRMOS:FUTURE
353S00831	3	IC,FDMF5804,IMVP-8,50A,PQFN31	Q7110,Q7130,Q7150	CPU_DRMOS:CURRENT

BOM_COST_GROUP=CPU & CHIPSET

DRAWING LAST_MODIFIED=Thu Oct 6 17:15:05 2016

PAGE TITLE
CPU & CHIPSET: CPU CORE VR (VCC)

Apple Inc.

DRAWING NUMBER 051-01506 SIZE D
REVISION 5.19.0
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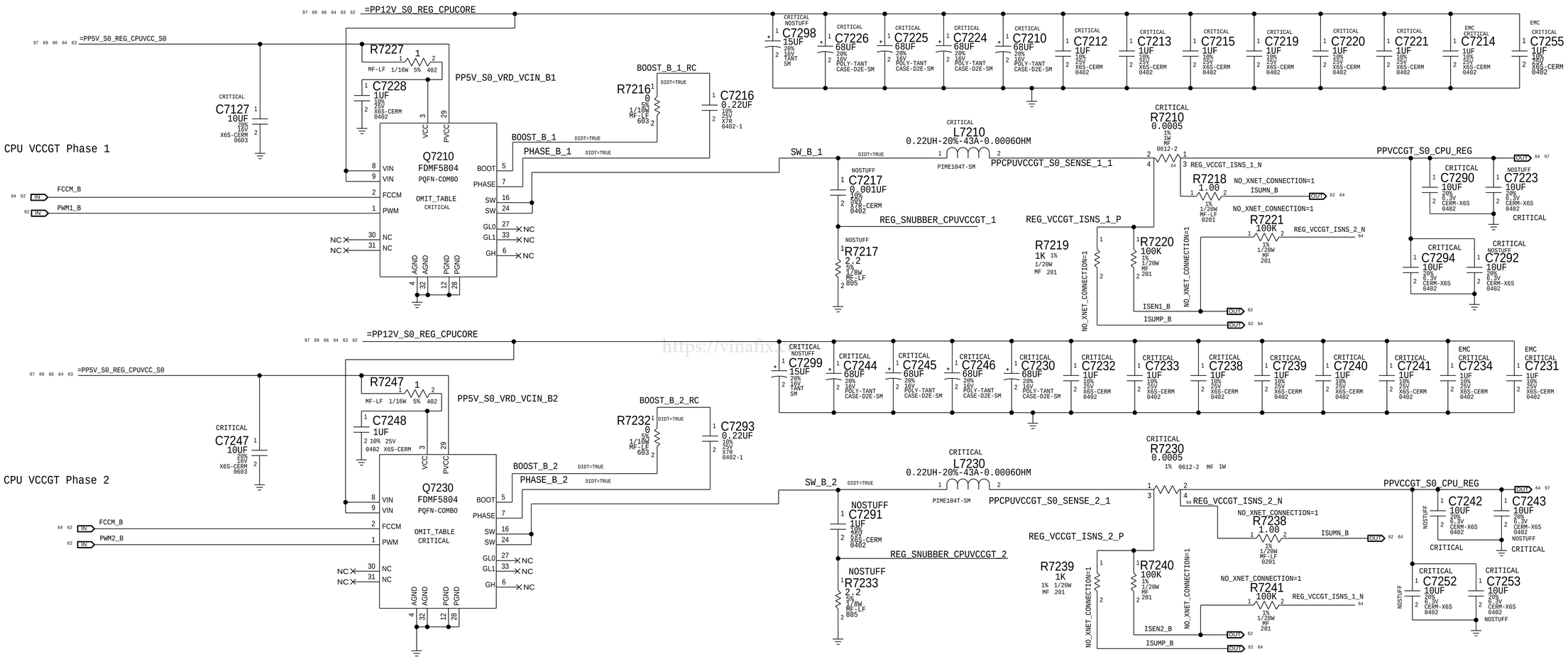
CPU VCCGT Regulator

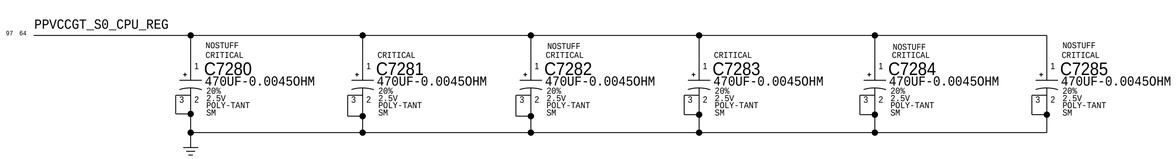
EDC = 51A

TDC = 37A



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S00519	2	IC,SIC621,IMVP-8,60A,PQFN31	Q7210,Q7230	CPU_DRMOS:FUTURE
353S00831	2	IC,FDMF5804,IMVP-8,50A,PQFN31	Q7210,Q7230	CPU_DRMOS:CURRENT

CPU VCCGT OUTPUT DECOUPLING



BOM_COST_GROUP=CPU & CHIPSET

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DRAWING LAST_MODIFIED=Thu Oct 6 17:15:05 2016

PAGE TITLE: CPU & CHIPSET: CPU CORE VR (VCCGT)

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DRAWING NUMBER: 051-01506 SIZE: D

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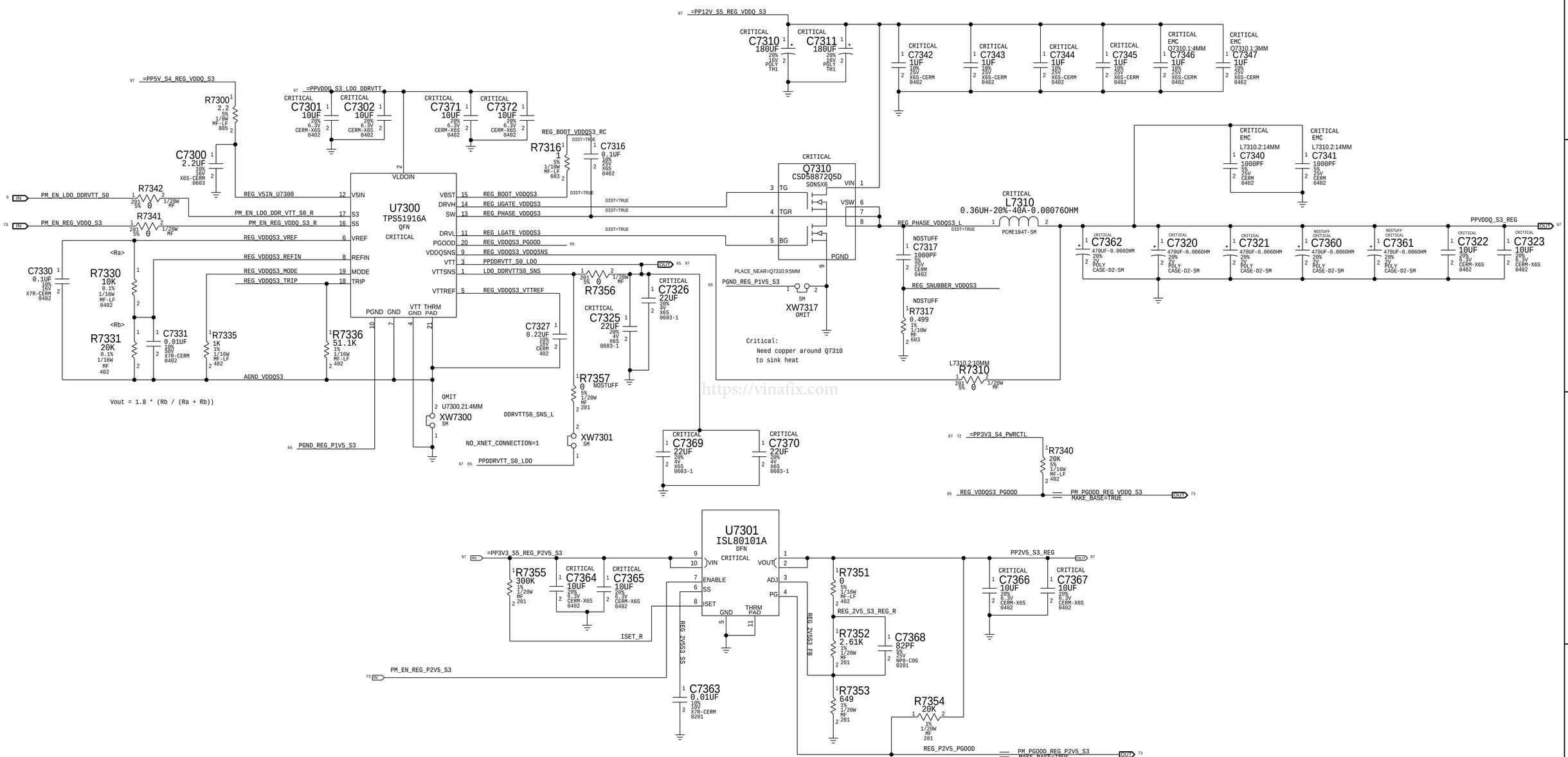
VDDQ S3 REGULATOR

VDDQ = 1.2V @ 12A (EDP)

VTT = 0.6V @ 3A (EDP)

VPP = 2.5V @ 1.1A (EDP)



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PAGE TITLE
CPU & CHIPSET: CPU VDDQ VR

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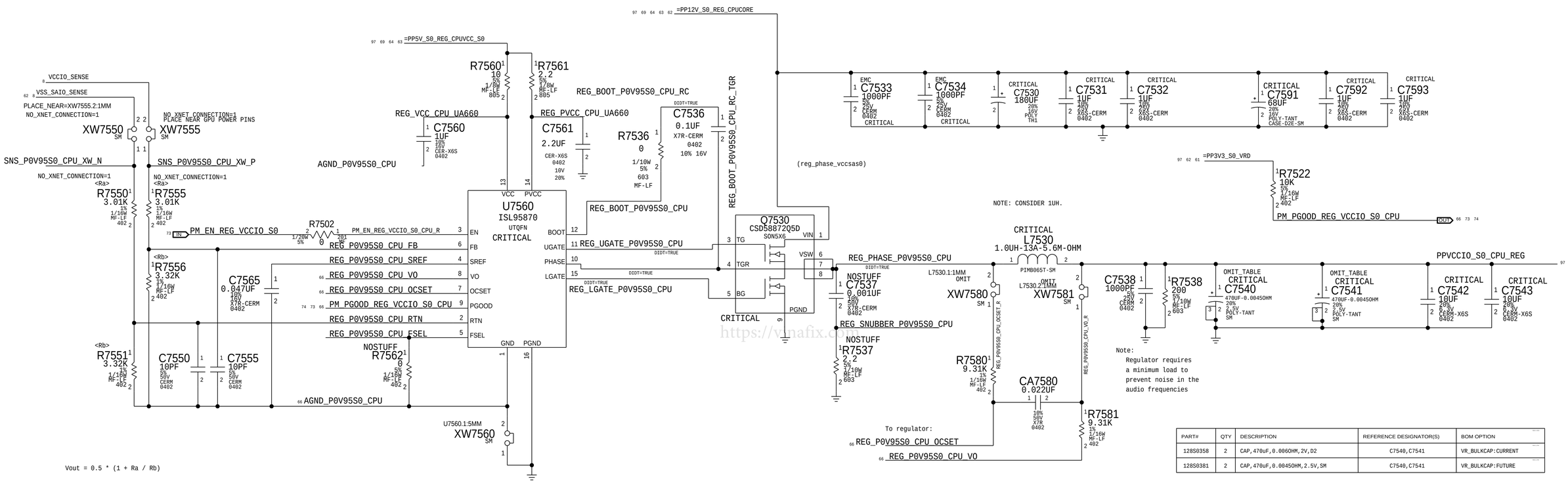
VCCIO S0 REGULATOR

0.95V @ 5.5A (EDP)



Vout = 0.5 * (1 + Ra / Rb)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
128S0358	2	CAP,470uF,0.0060HM,2V,D2	C7540,C7541	VR_BULKCAP:CURRENT
128S0381	2	CAP,470uF,0.00450HM,2.5V,SM	C7540,C7541	VR_BULKCAP:FUTURE

BOM_COST_GROUP=CPU & CHIPSET

DRAWING LAST_MODIFIED=Thu Oct 6 17:15:05 2016

PAGE TITLE
CPU & CHIPSET: CPU VCCIO VR

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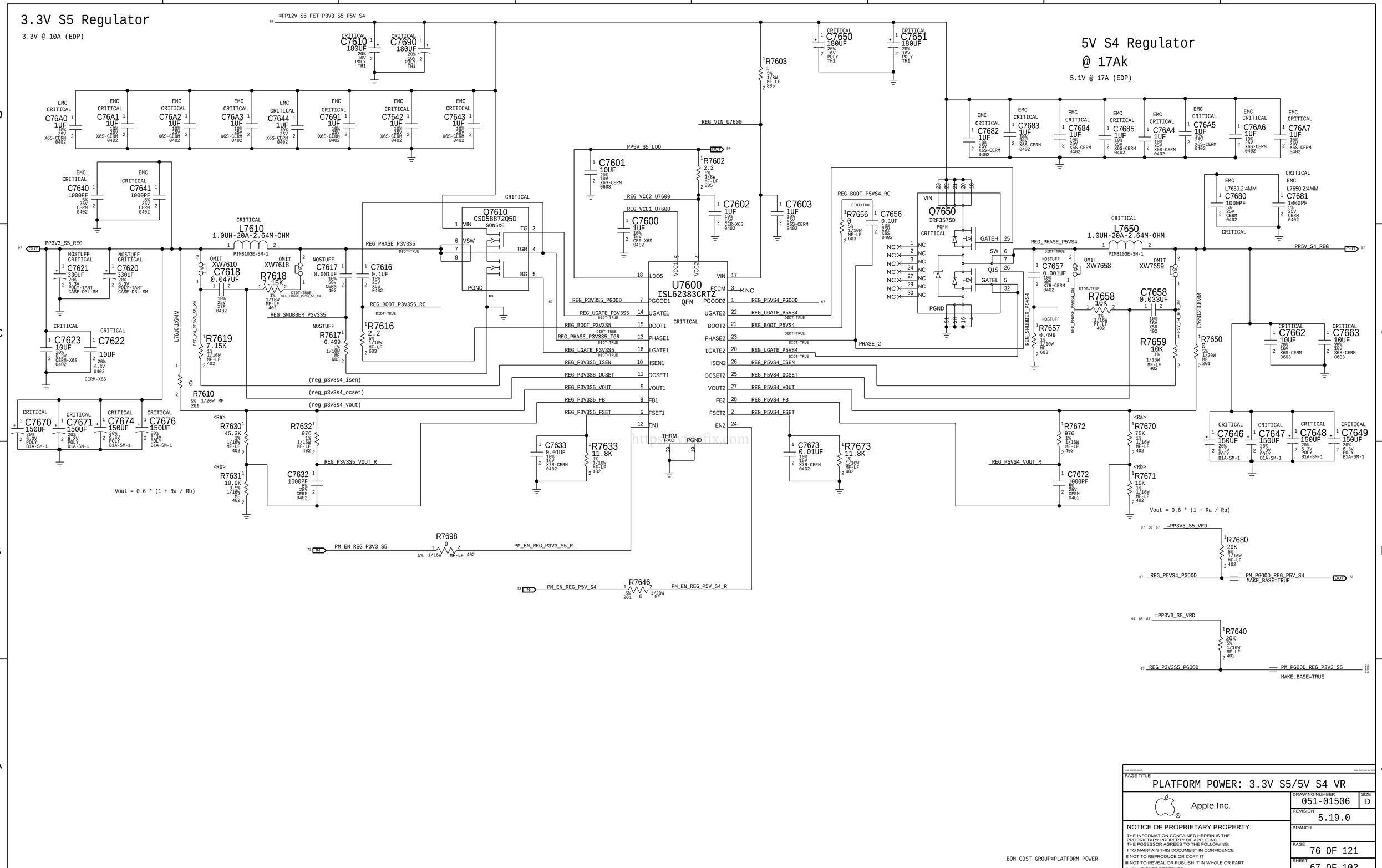
3.3V S5 Regulator
3.3V @ 10A (EDP)
5V S4 Regulator
@ 17Ak
5.1V @ 17A (EDP)
=PP12V_S5_FET_P3V3_S5_P5V_S4
PP3V3_S5_REG
PP5V_S5_LDO
REG_VIN_U7600
REG_VCC2_U7600
REG_VCC1_U7600
REG_PHASE_P3V3S5
REG_BOOT_P3V3S5_RC
REG_SNUBBER_P3V3S5
REG_BOOT_P5VS4_RC
REG_PHASE_P5VS4
PP5V_S4_REG
U7600
ISL62383CRTZ
QFN
Q7610
CSD5887Q5D
Q7650
IRF3575D
PQFN
L7610
1.0UH-20A-2.64M-OHM
L7650
1.0UH-20A-2.64M-OHM
PIMB103E-SM-1
(reg_p3v3s4_isen)
(reg_p3v3s4_ocset)
(reg_p3v3s4_vout)
REG_P3V3S5_VOUT_R
REG_P5VS4_VOUT_R
Vout = 0.6 * (1 + Ra / Rb)
PM_EN_REG_P3V3_S5
PM_EN_REG_P3V3_S5_R
PM_EN_REG_P5V_S4
PM_EN_REG_P5V_S4_R
=PP3V3_S5_VRD
REG_P5VS4_PGOOD
PM_PGOOD_REG_P5V_S4
MAKE_BASE=TRUE
REG_P3V3S5_PGOOD
PM_PGOOD_REG_P3V3_S5
MAKE_BASE=TRUE
BOM_COST_GROUP=PLATFORM POWER
PAGE TITLE
PLATFORM POWER: 3.3V S5/5V S4 VR
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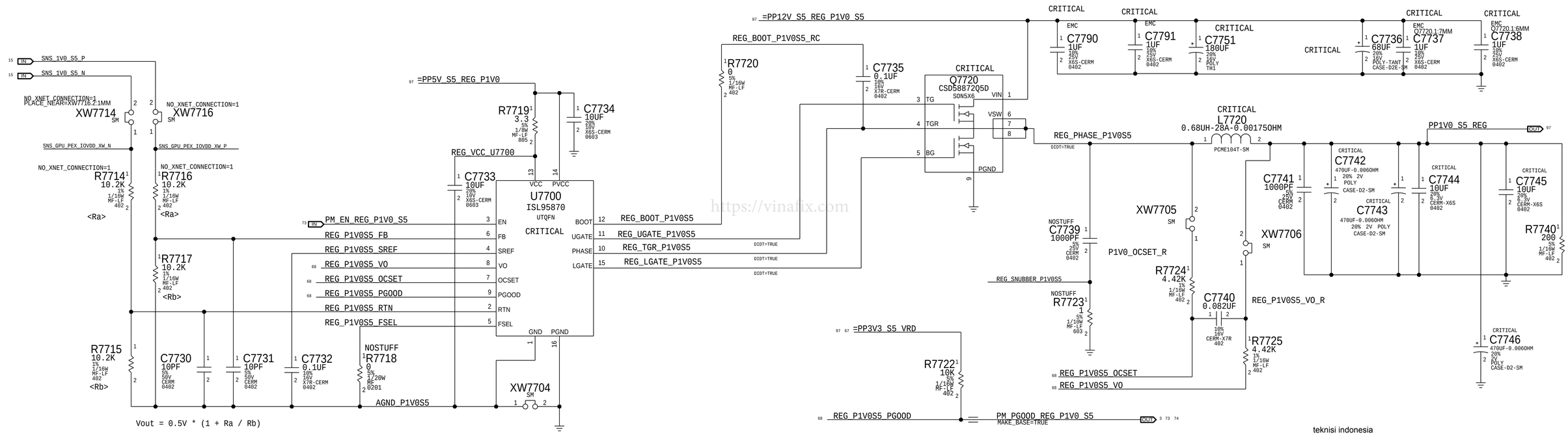

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teknisi indonesia

PAGE TITLE
CPU & CHIPSET: PCH 1V0 & 1V8 VR

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DRAWING NUMBER 051-01506
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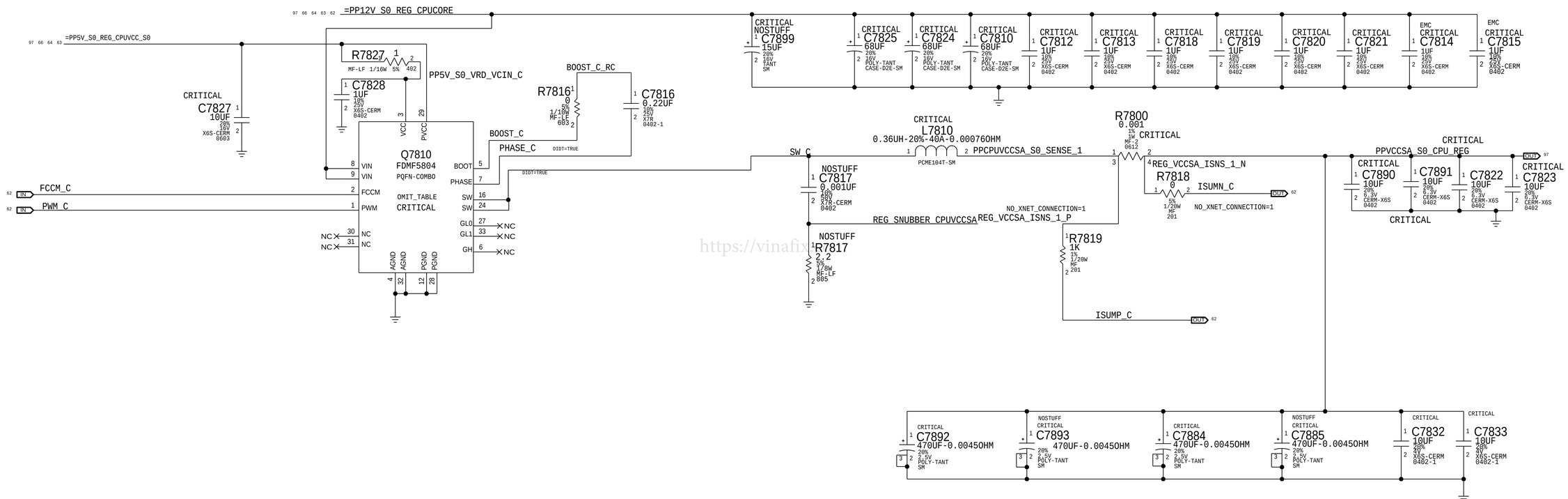
CPU VCCSA Regulator

EDC = 11.1A

TDC = 10A



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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S00519	1	IC,SIC621,IMVP-8,60A,PQFN31	Q7810	CPU_DRMOS:FUTURE
353S00831	1	IC,FDMF5804,IMVP-8,50A,PQFN31	Q7810	CPU_DRMOS:CURRENT

BOM_COST_GROUP=CPU & CHIPSET

DRAWING LAST_MODIFIED=Thu Oct 6 17:15:06 2016

PAGE TITLE

CPU & CHIPSET: CPU CORE VR (VCCSA)

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DRAWING NUMBER 051-01506

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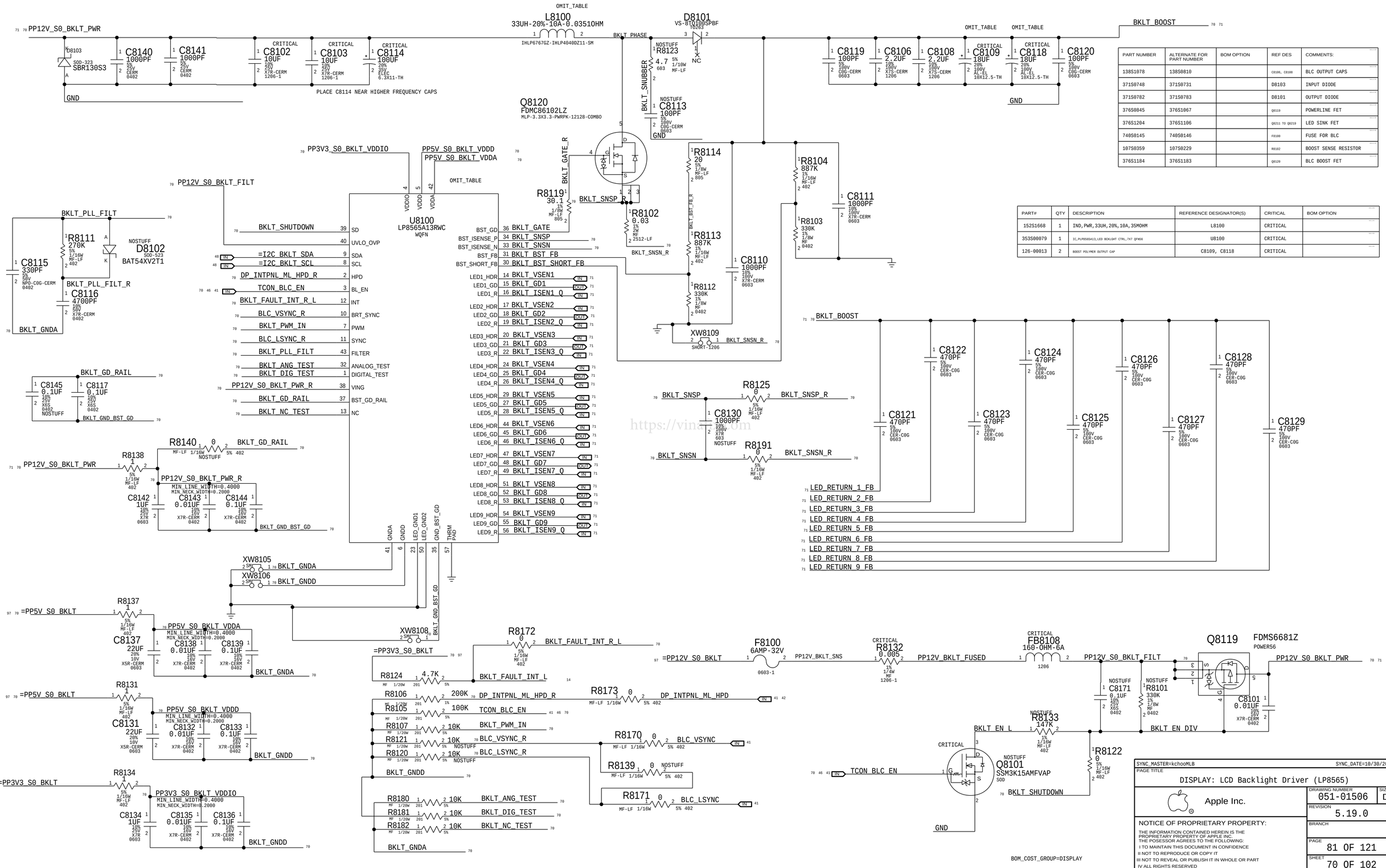
OMIT/table L8100 due to late sourcing change, did not want footprint change
Add 152s1668 (Cyntec) directly for next program



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S1078	138S0810		C8106, C8108	BLC OUTPUT CAPS
371S0748	371S0731		D8103	INPUT DIODE
371S0782	371S0783		D8101	OUTPUT DIODE
376S0845	376S1067		Q8119	POWERLINE FET
376S1204	376S1106		Q8211 TO Q8219	LED SINK FET
740S0145	740S0146		F8100	FUSE FOR BLC
107S0359	107S0229		R8102	BOOST SENSE RESISTOR
376S1184	376S1183		Q8120	BLC BOOST FET

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S1668	1	IND,PWR,33UH,20%,10A,35MOHM	L8100	CRITICAL	
353S00079	1	IC,PLP8565A13,LED BCKLGHT CTRL,7X7 QFN56	U8100	CRITICAL	
126-00013	2	BOOST POLYMER OUTPUT CAP	C8109, C8118	CRITICAL	

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SYNC_MASTER=kchooMLB SYNC_DATE=10/30/2015

PAGE TITLE

DISPLAY: LCD Backlight Driver (LP8565)

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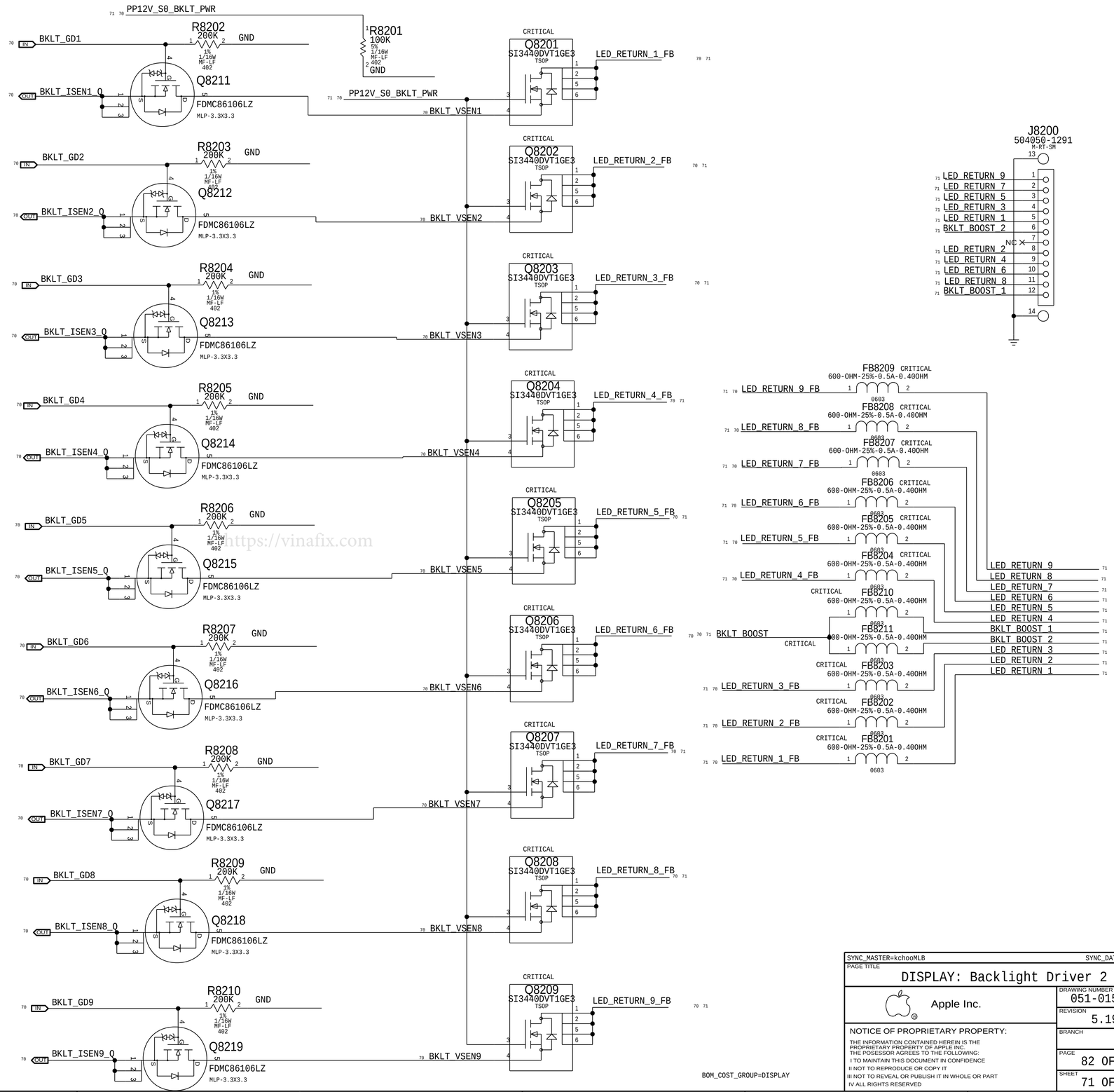
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1256	376S1073		ALL	Short Protection FET
155S0831	155S0797		ALL	FB8201 TO FB8211



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SYNC_MASTER=kchooMLB SYNC_DATE=10/30/2015

PAGE TITLE
DISPLAY: Backlight Driver 2

Apple Inc.

DRAWING NUMBER 051-01506 SIZE D
REVISION 5.19.0
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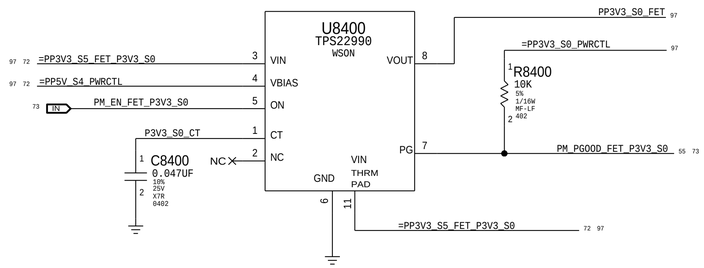
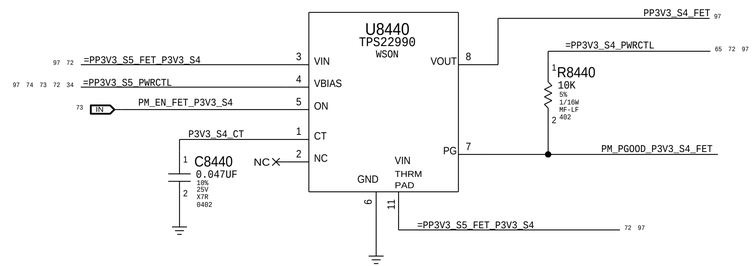
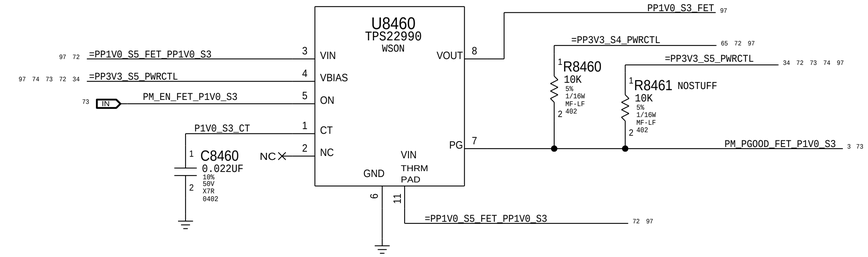
3.3V S0 FET (? PK / 2.0A AVG)
RAMP RATE = ~1.56V/MS



3.3V S4 FET (2.7A PK / 2.0A AVG)
RAMP RATE = ~1.74V/MS

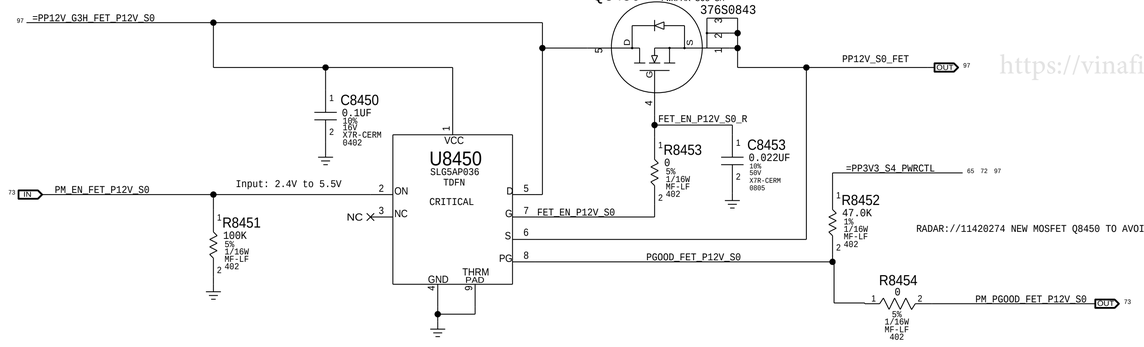


1.0V S3 FET (??A PK / 0.27A AVG)
RAMP RATE = ~3.0V/MS



12V S0 FET

Max avg current: 20.4 A (BUDGET)
Max peak current: 24.1 A (BUDGET)



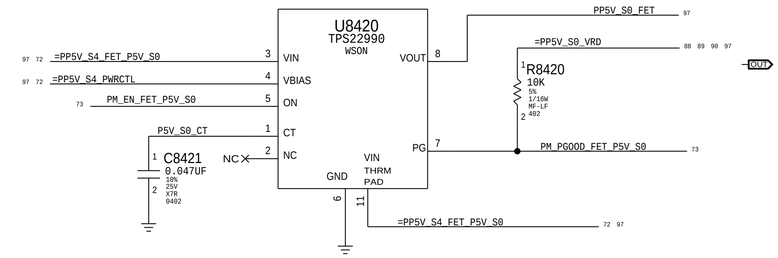
RADAR://11420274 NEW MOSFET Q8450 TO AVOID 50A 100US PULSE ON 12V S0.

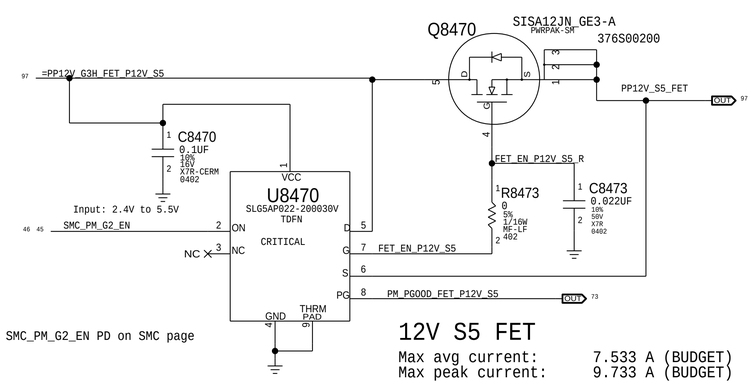
RADAR://10865139 U8470 ENSURES S5_PWRGD ISN'T ASSERTED AFTER HARD SHUTDOWN.

https://vinafix.com

5V S0 FET

Max avg current: 2.7 A (BUDGET)
Max peak current: 3.9 A (BUDGET)
RAMP RATE = ~1.46V/MS





SMC_PM_G2_EN PD on SMC page

12V S5 FET

Max avg current: 7.533 A (BUDGET)
Max peak current: 9.733 A (BUDGET)

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=kchooMLB	SYNC_DATE=10/30/2015
PAGE TITLE: PLATFORM POWER: FET-Controlled S0 and S4	
Apple Inc.	DRAWING NUMBER: 051-01506 — SIZE: D
	REVISION: 5.19.0
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	PAGE: 84 OF 121
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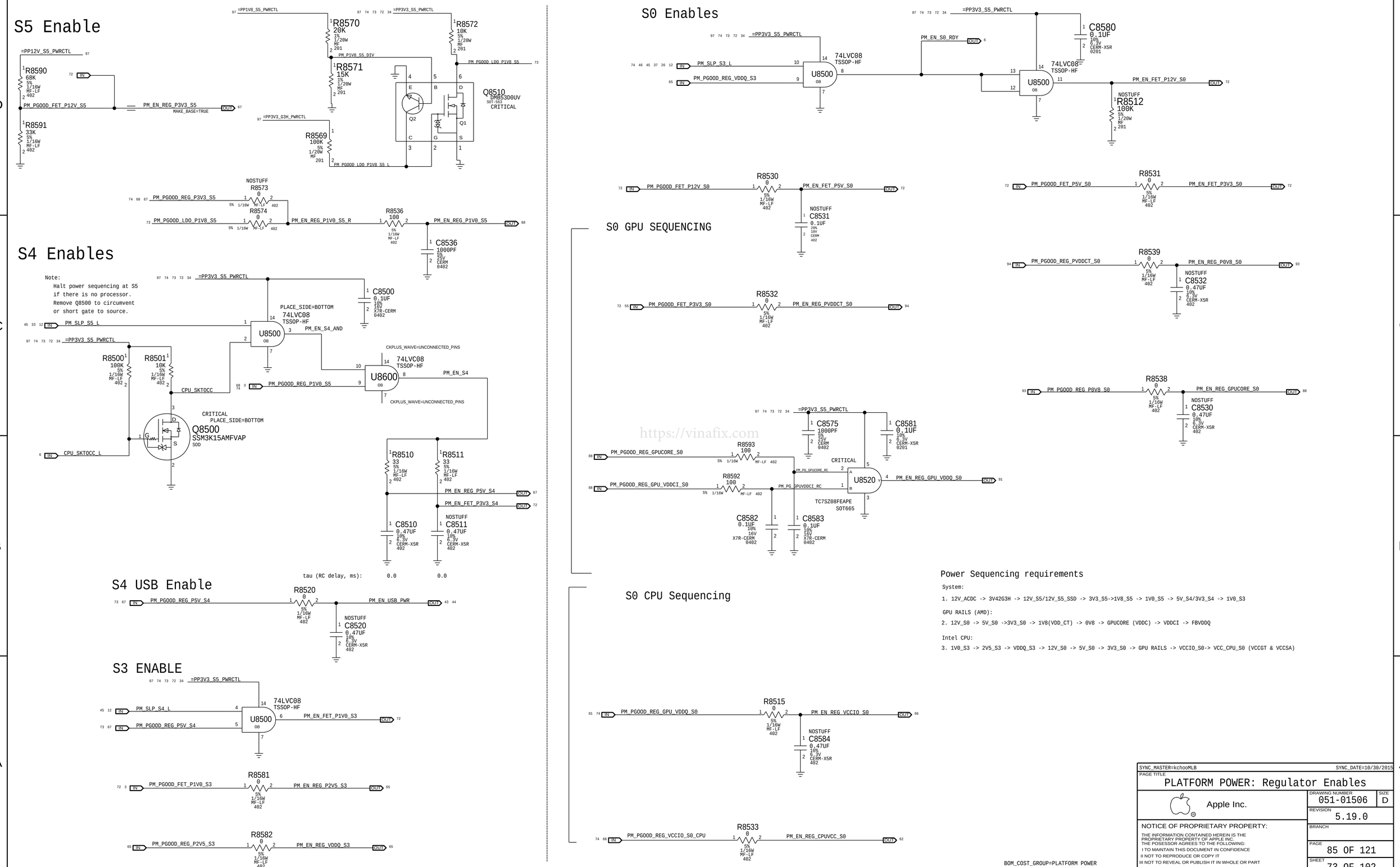
S5 Enable
S4 Enables
S4 USB Enable
S3 ENABLE
S0 Enables
S0 GPU SEQUENCING
S0 CPU Sequencing
Power Sequencing requirements
System:
1. 12V_ACDC -> 3V42G3H -> 12V_S5/12V_S5_SSD -> 3V3_S5->1V8_S5 -> 1V0_S5 -> 5V_S4/3V3_S4 -> 1V0_S3
GPU RAILS (AMD):
2. 12V_S0 -> 5V_S0 ->3V3_S0 -> 1V8(VDD_CT) -> 0V8 -> GPUCORE (VDDC) -> VDDCI -> FBVDDQ
Intel CPU:
3. 1V0_S3 -> 2V5_S3 -> VDDQ_S3 -> 12V_S0 -> 5V_S0 -> 3V3_S0 -> GPU RAILS -> VCCIO_S0-> VCC_CPU_S0 (VCCGT & VCCSA)
Note:
Halt power sequencing at S5
if there is no processor.
Remove Q8500 to circumvent
or short gate to source.
tau (RC delay, ms): 0.0 0.0
https://vinafix.com
BOM_COST_GROUP=PLATFORM POWER
SYNC_MASTER=kchooMLB
SYNC_DATE=10/30/2015
PAGE TITLE
PLATFORM POWER: Regulator Enables
Apple Inc.
DRAWING NUMBER
051-01506
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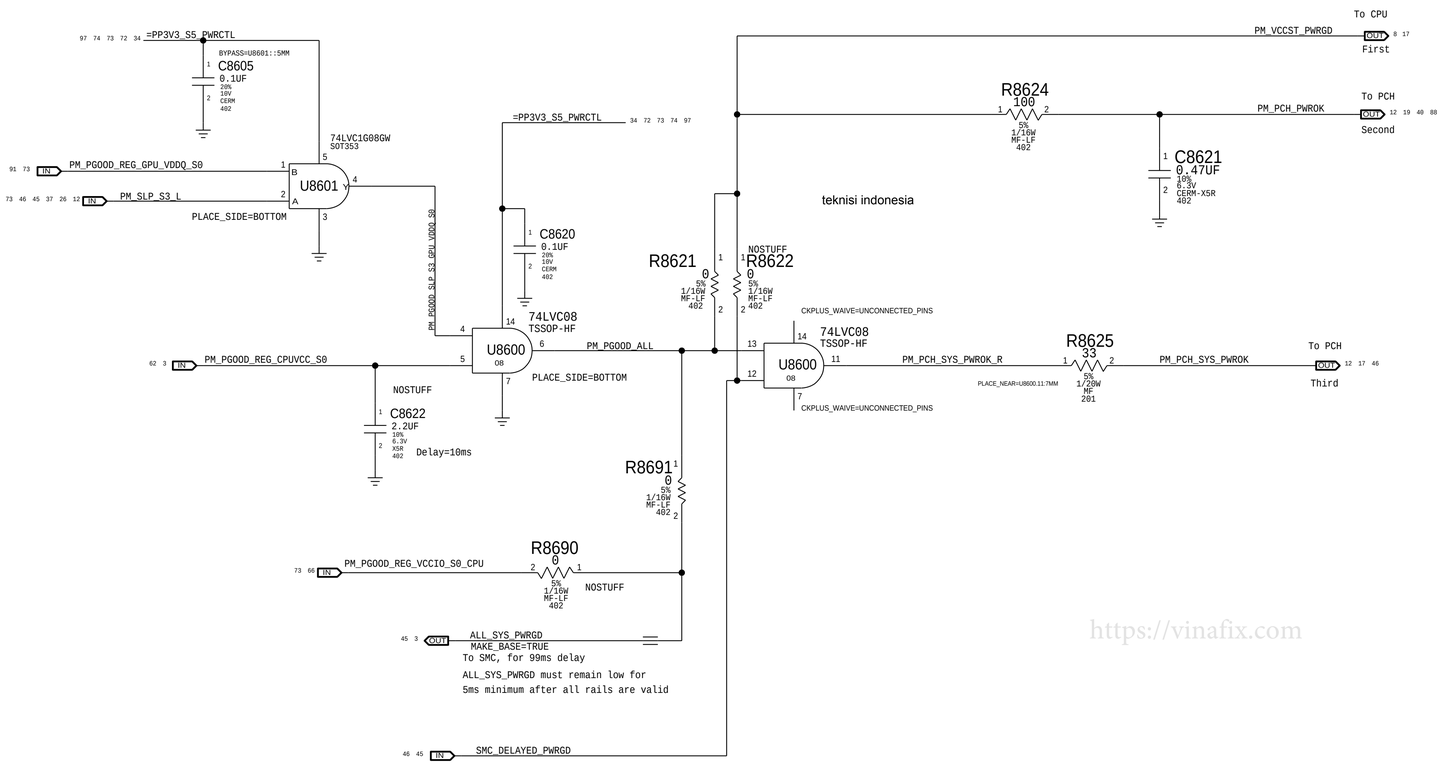
ALL_SYS_PWRGD,PCH_PWROK & SYS_PWROK Generation

PCH Power Goods



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Resume Reset

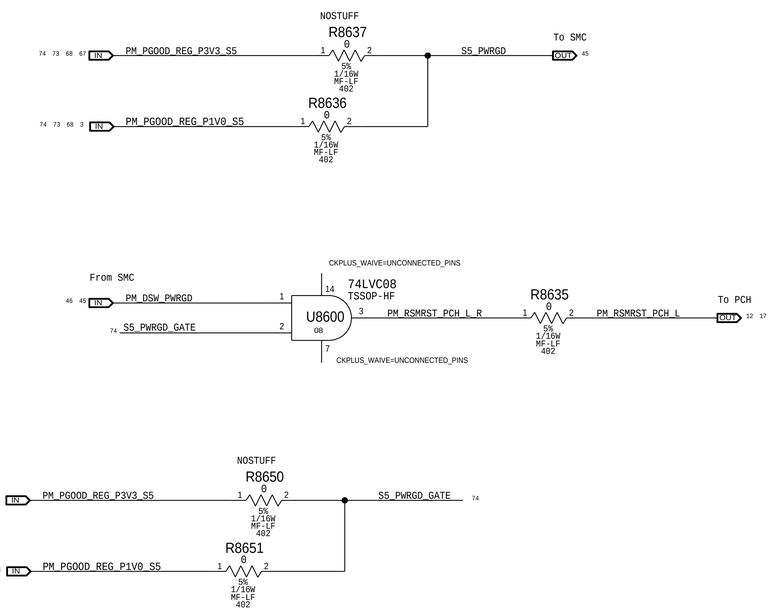
Intel Doc# 29517 Maho Bay PDG, Section 22.13
Intel Doc# 29562 Panther Point EDS, Section 8.7 and 8.8

Note:
THE IMAC J135 DESIGNS DOES NOT SUPPORT DEEP SX MODES SO BOTH DPWROK AND RSMRST# signals are shorted together

Requirements:
Power on:
Asserted at least 10 ms after all suspend well power is valid
Power off or loss of AC:
Transition to 0.8V or less before VccSUS3_3 drops to 2.90 V
to allow PCH to switch suspend well to battery without excessive loading

Method:
The SMC guarantees proper assertion and de-assertion of RSMRST# for normal operation via PM_DSW_PWRGD.

RSMRST# is asserted when power good from regulator is de-asserted in the event AC is lost. Power good de-assertion should happen quickly enough to meet Intel spec.



BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=kchooMLB SYNC_DATE=10/30/2015

PAGE TITLE
PLATFORM POWER: PM Power Good

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POLARITY SWAP NOT SUPPORTED BY SKYLAKE
ALL LANES ARE ALSO REVERSED, SEE ALIASES ON CSA 112

SEE OMIT TABLE ON CSA 96 FOR STUFFING OPTIONS
NOTE: ELLESMERE'S PEG WIDTH IS X16, BAFFIN X8

75 PEG_R2D_P<8>	C8720	0.22UF	GND_VOID=TRUE	PEG_R2D_C_P<8>	99
75 PEG_R2D_N<8>	C8721	0.22UF	GND_VOID=TRUE	PEG_R2D_C_N<8>	99
75 PEG_R2D_P<1>	C8722	0.22UF	GND_VOID=TRUE	PEG_R2D_C_P<1>	99
75 PEG_R2D_N<1>	C8723	0.22UF	GND_VOID=TRUE	PEG_R2D_C_N<1>	99
75 PEG_R2D_P<2>	C8724	0.22UF	GND_VOID=TRUE	PEG_R2D_C_P<2>	99
75 PEG_R2D_N<2>	C8725	0.22UF	GND_VOID=TRUE	PEG_R2D_C_N<2>	99
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75 PEG_R2D_N<3>	C8727	0.22UF	GND_VOID=TRUE	PEG_R2D_C_N<3>	99
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U8700
ELLSMERE-XTA
BGA
100-CK4788-ES
SYM 2 OF 13
PCIEXPRESS

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NOSTUFF R8702 0 1 2 1/20W 5% MF 201
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L8700
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PLACE IND & CAPS ALONG
EDGE OF GPU

C8790	10UF 20% 4V X6S 0402	C8791	4.7UF 20% 6.3V X6S 0402
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PLACE THESE CAPS UNDER GPU

97 75 =PP0V8_S0_GPU_PCIEVDDC

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C8794	4.7UF 20% 6.3V X6S 0402	C8795	4.7UF 20% 6.3V X6S 0402
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PLACE THESE CAPS UNDER GPU

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SYNC_MASTER=PETE SYNC_DATE=03/31/2016

PAGE TITLE
GFX: GPU PCIE INTF

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REVISION 5.19.0
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SHEET 75 OF 102

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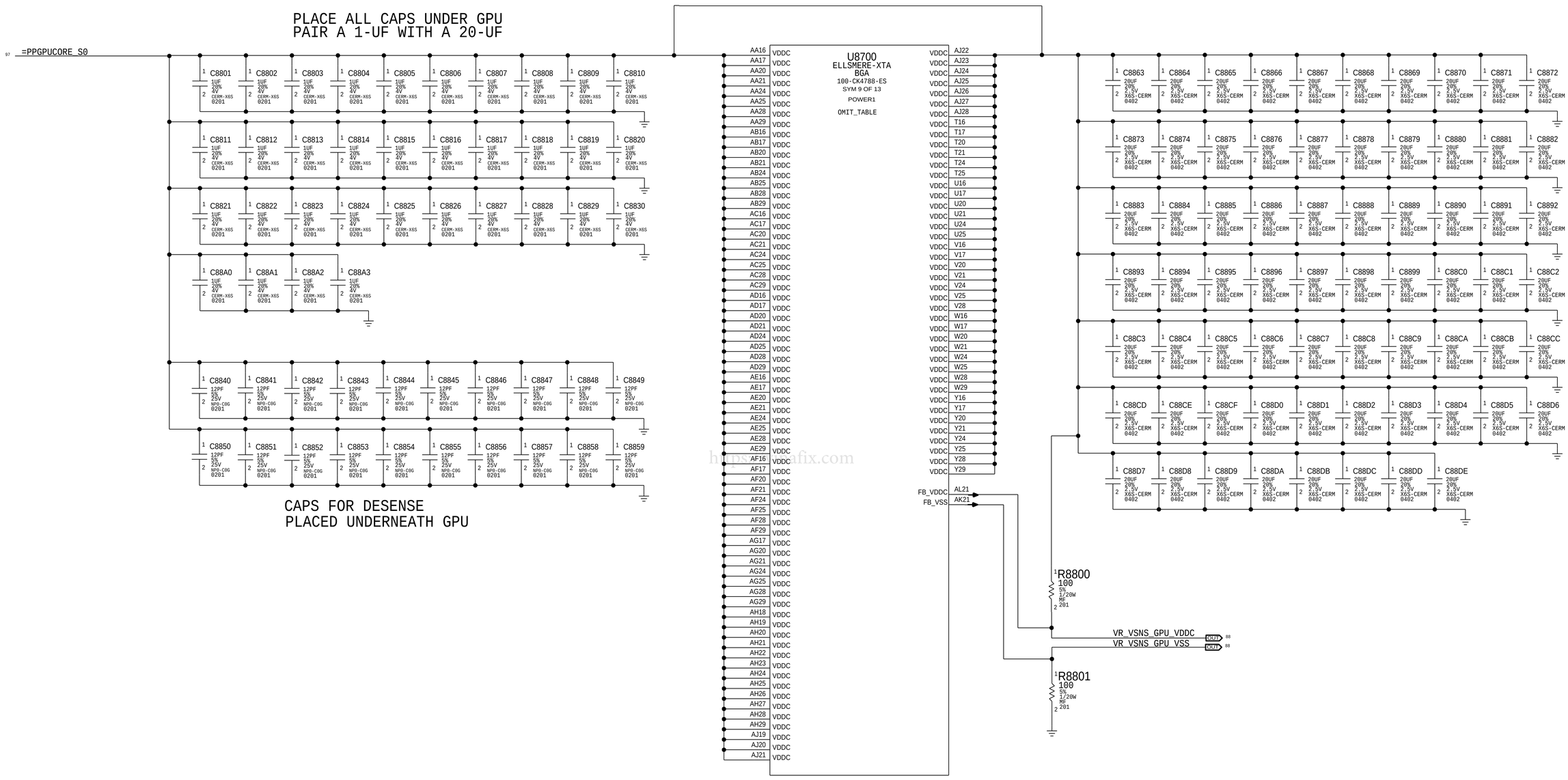
GPU VDDC DECOUPLING



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GPU VMEMIO/VDDCI DECOUPLING

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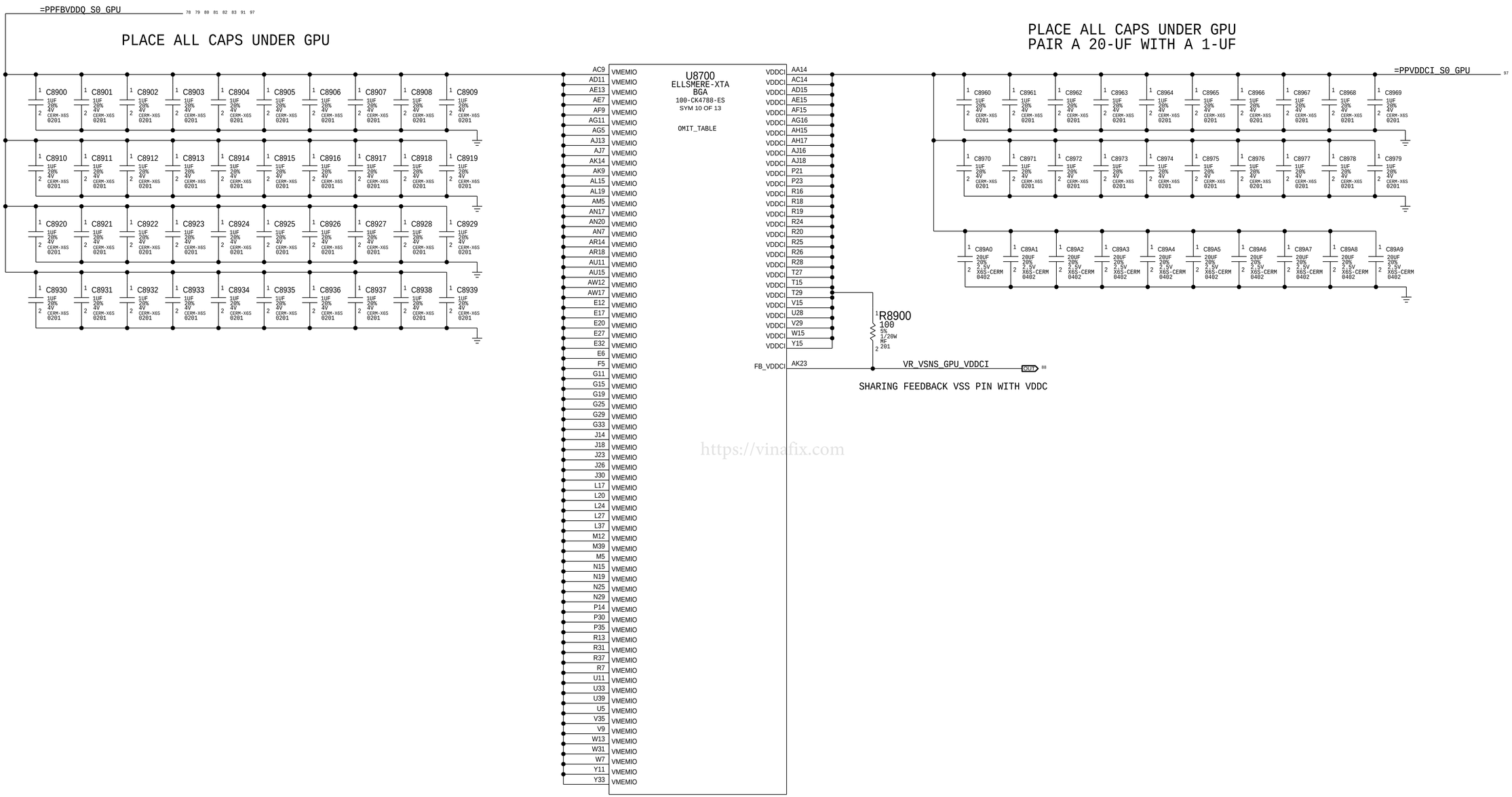

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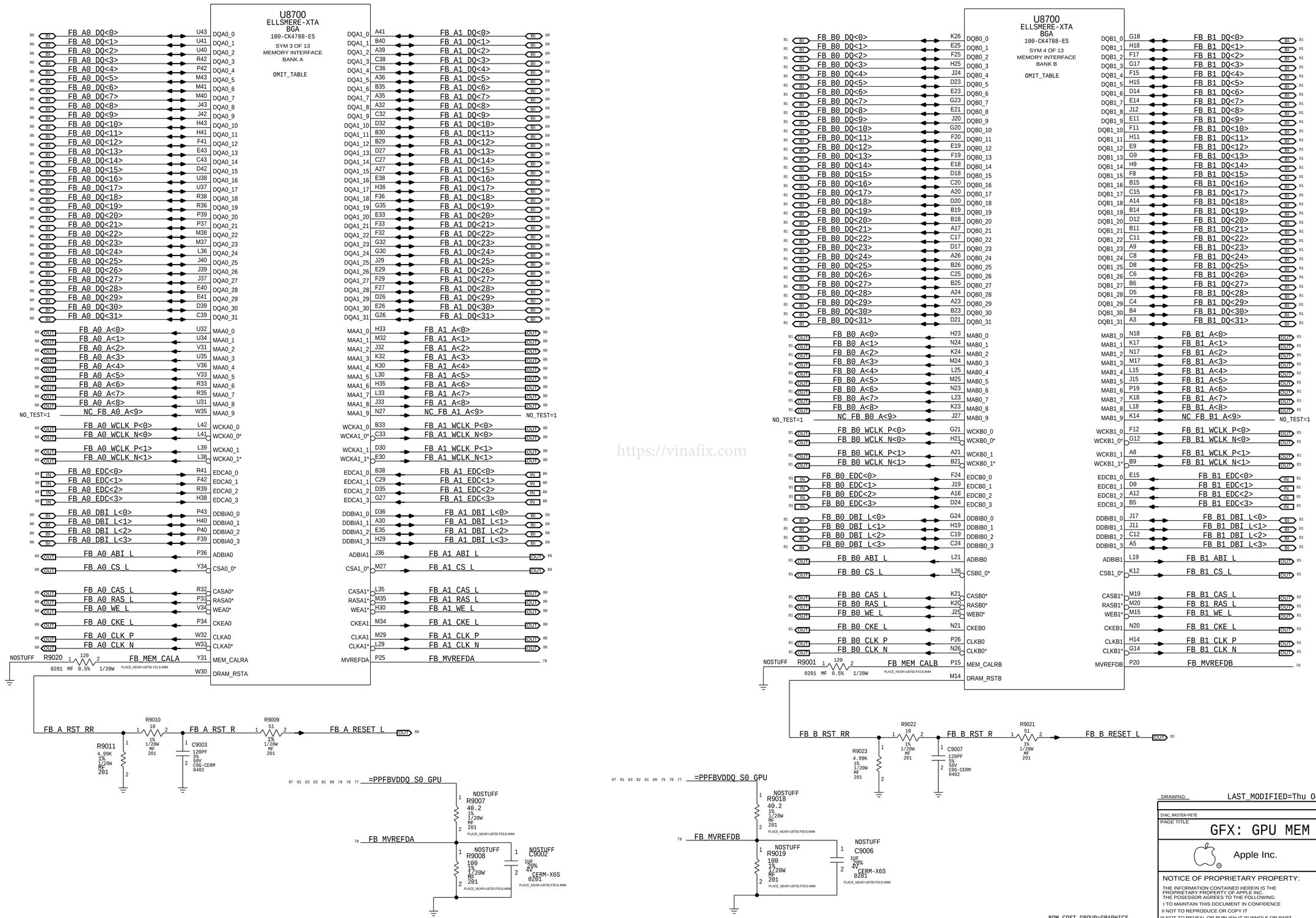

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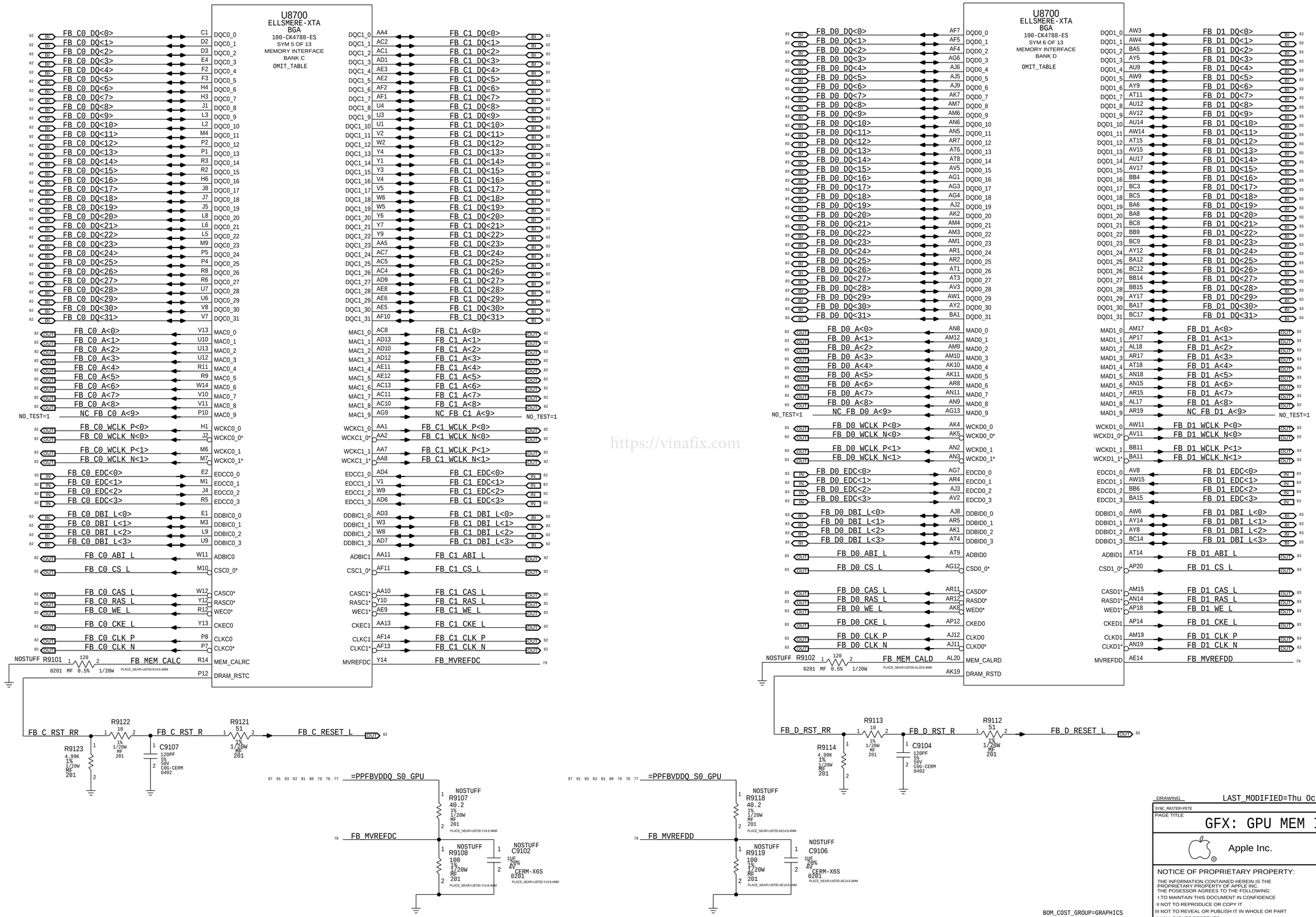

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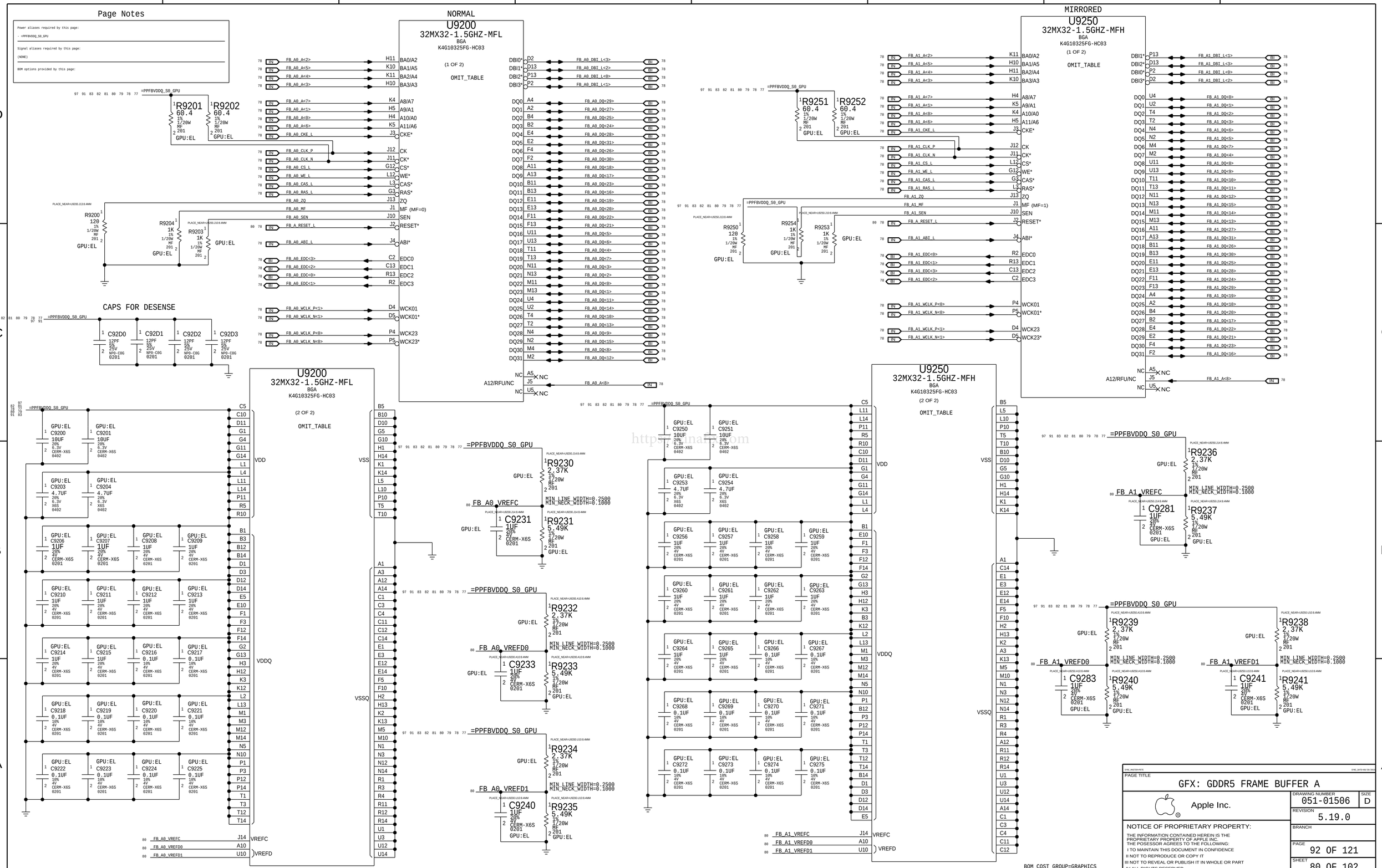
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Apple Inc.
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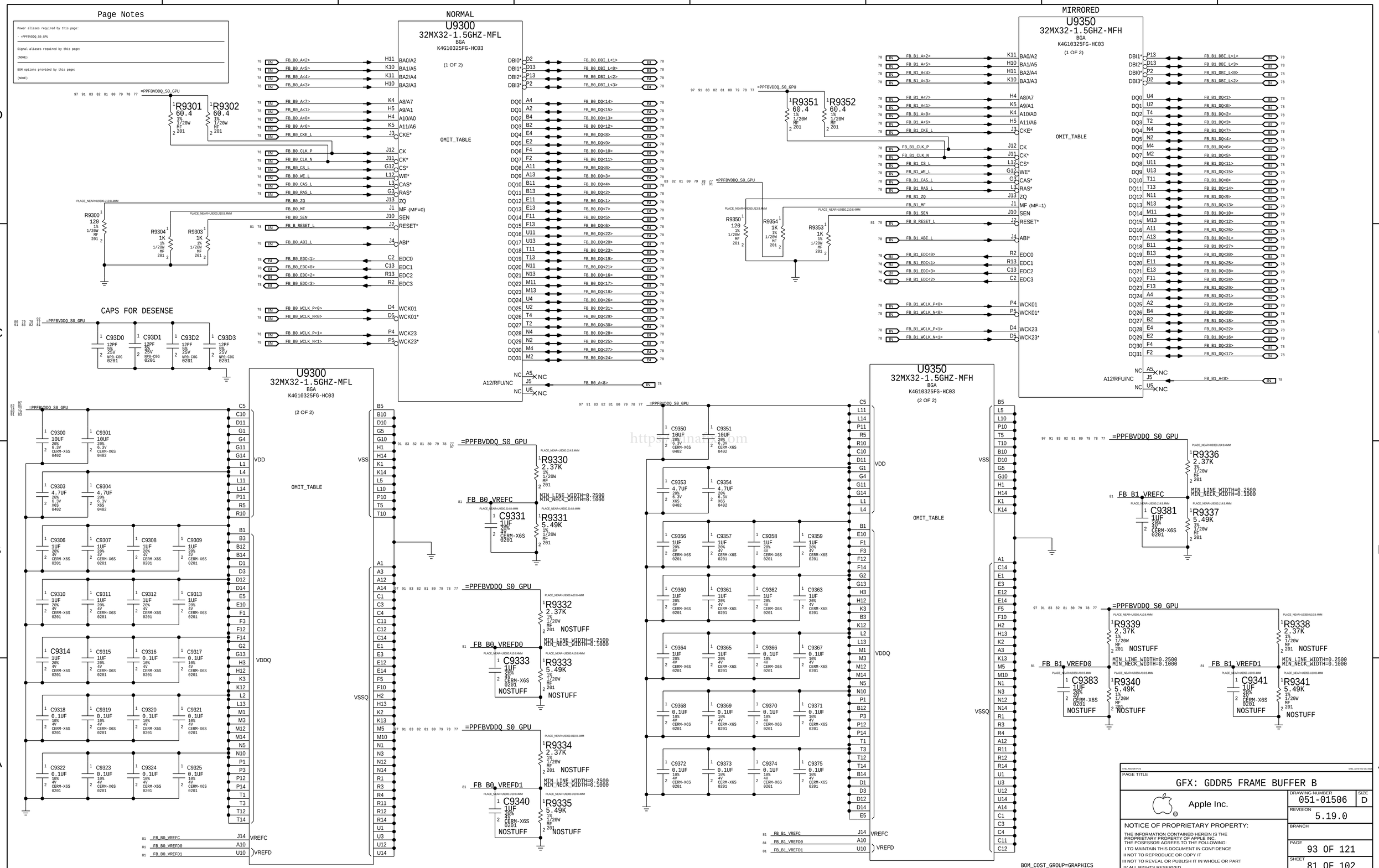
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32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(1 OF 2)
OMIT_TABLE
MIRRORED
U9350
32MX32-1.5GHZ-MFH
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(1 OF 2)
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CAPS FOR DESENSE
U9300
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BGA
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BGA
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(2 OF 2)
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R9301 60.4 1% 1/20W MF 201
R9302 60.4 1% 1/20W MF 201
R9351 60.4 1% 1/20W MF 201
R9352 60.4 1% 1/20W MF 201
R9300 120 1% 1/20W MF 201
R9304 1K 1% 1/20W MF 201
R9303 1K 1% 1/20W MF 201
R9350 120 1% 1/20W MF 201
R9354 1K 1% 1/20W MF 201
R9353 1K 1% 1/20W MF 201
C93D0 12PF 5% 25V NP0-C0G 0201
C93D1 12PF 5% 25V NP0-C0G 0201
C93D2 12PF 5% 25V NP0-C0G 0201
C93D3 12PF 5% 25V NP0-C0G 0201
C9300 10UF 20% 6.3V CERM-X6S 0402
C9301 10UF 20% 6.3V CERM-X6S 0402
C9303 4.7UF 20% 6.3V X6S 0402
C9304 4.7UF 20% 6.3V X6S 0402
C9306 1UF 20% 4V CERM-X6S 0201
C9307 1UF 20% 4V CERM-X6S 0201
C9308 1UF 20% 4V CERM-X6S 0201
C9309 1UF 20% 4V CERM-X6S 0201
C9310 1UF 20% 4V CERM-X6S 0201
C9311 1UF 20% 4V CERM-X6S 0201
C9312 1UF 20% 4V CERM-X6S 0201
C9313 1UF 20% 4V CERM-X6S 0201
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C9316 0.1UF 10% 4V CERM-X6S 0201
C9317 0.1UF 10% 4V CERM-X6S 0201
C9318 0.1UF 10% 4V CERM-X6S 0201
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R9332 2.37K 1% 1/20W MF 201 NOSTUFF
R9333 5.49K 1% 1/20W MF 201 NOSTUFF
C9333 1UF 20% 4V CERM-X6S 0201 NOSTUFF
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C9350 10UF 20% 6.3V CERM-X6S 0402
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C9383 1UF 20% 4V CERM-X6S 0201 NOSTUFF
R9340 5.49K 1% 1/20W MF 201 NOSTUFF
C9341 1UF 20% 4V CERM-X6S 0201 NOSTUFF
R9341 5.49K 1% 1/20W MF 201 NOSTUFF
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FB_B1_VREFD1
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VDDQ
VSS
VSSQ
VREFC
VREFD
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GFX: GDDR5 FRAME BUFFER B
Apple Inc.
DRAWING NUMBER
051-01506
SIZE
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REVISION
5.19.0
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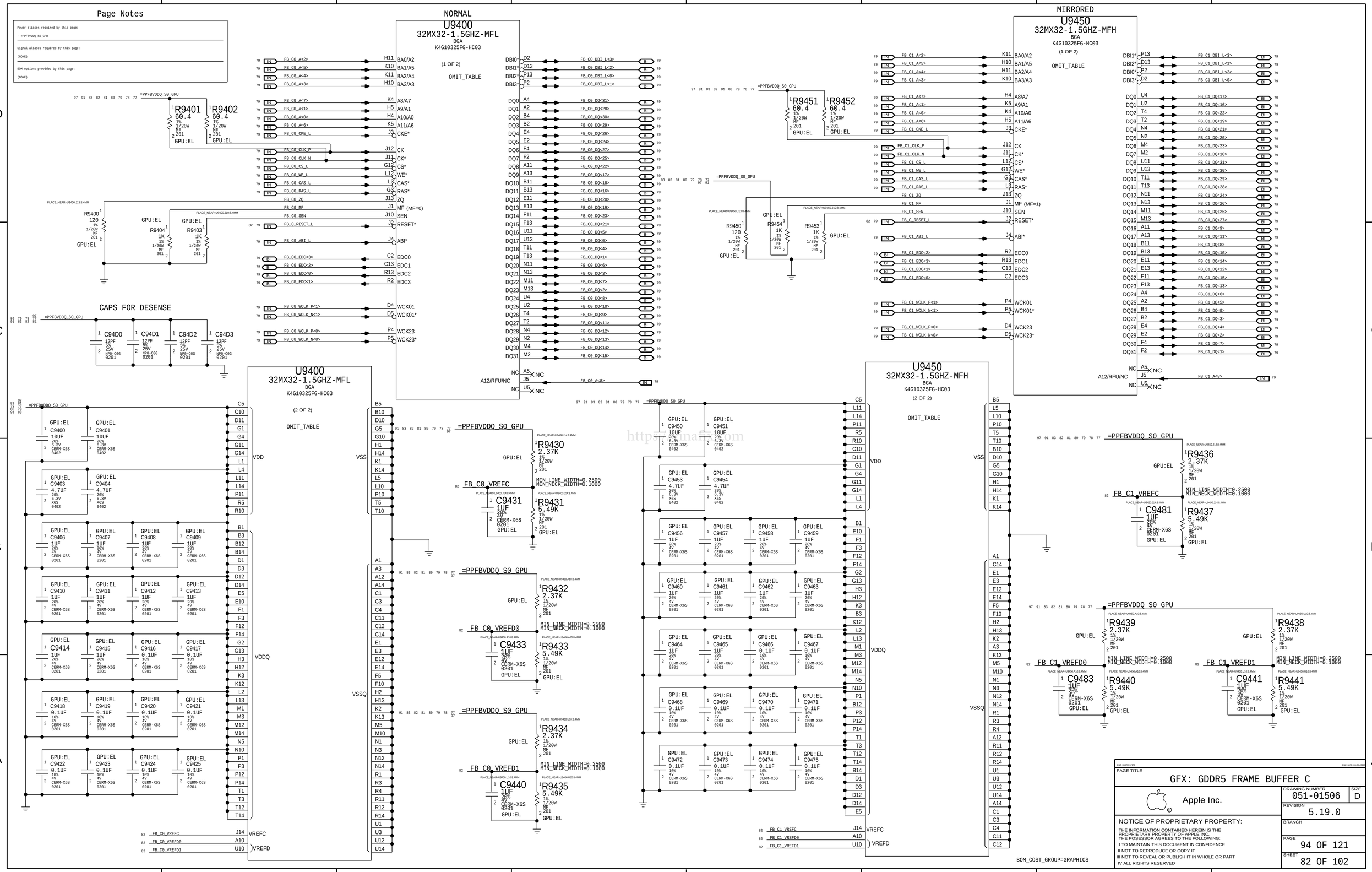
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Signal aliases required by this page:
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BOM options provided by this page:
(NONE)
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U9400
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(1 OF 2)
OMIT_TABLE
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U9450
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CAPS FOR DESENSE
U9400
32MX32-1.5GHZ-MFL
BGA
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OMIT_TABLE
U9450
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(2 OF 2)
OMIT_TABLE
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R9402 60.4 1% 1/20W MF 201 GPU:EL
R9451 60.4 1% 1/20W MF 201 GPU:EL
R9452 60.4 1% 1/20W MF 201 GPU:EL
R9400 120 1% 1/20W MF 201 GPU:EL
R9404 1K 1% 1/20W MF 201 GPU:EL
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R9450 120 1% 1/20W MF 201 GPU:EL
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R9453 1K 1% 1/20W MF 201 GPU:EL
C94D0 12PF 5% 25V NP0-C0G 0201
C94D1 12PF 5% 25V NP0-C0G 0201
C94D2 12PF 5% 25V NP0-C0G 0201
C94D3 12PF 5% 25V NP0-C0G 0201
VDD
VDDQ
VSS
VSSQ
VREFC
VREFD
R9430 2.37K 1% 1/20W MF 201 GPU:EL
R9431 5.49K 1% 1/20W MF 201 GPU:EL
R9432 2.37K 1% 1/20W MF 201 GPU:EL
R9433 5.49K 1% 1/20W MF 201 GPU:EL
R9434 2.37K 1% 1/20W MF 201 GPU:EL
R9435 5.49K 1% 1/20W MF 201 GPU:EL
R9436 2.37K 1% 1/20W MF 201 GPU:EL
R9437 5.49K 1% 1/20W MF 201 GPU:EL
R9439 2.37K 1% 1/20W MF 201 GPU:EL
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GFX: GDDR5 FRAME BUFFER C
Apple Inc.
DRAWING NUMBER
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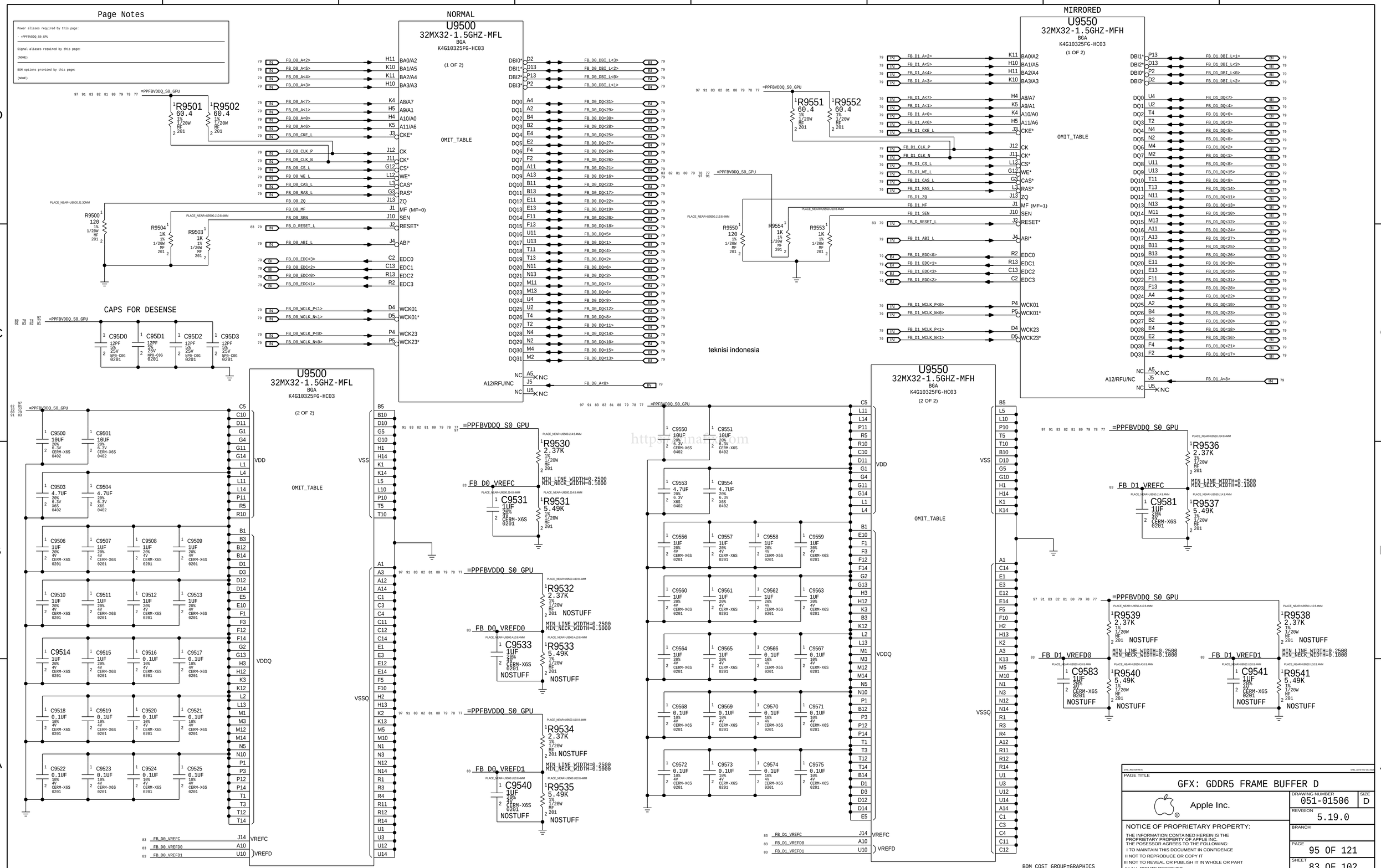
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32MX32-1.5GHZ-MFL
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BGA
K4G10325FG-HC03
(2 OF 2)
OMIT_TABLE
teknisi indonesia
http://manuals.info.com
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Apple Inc.
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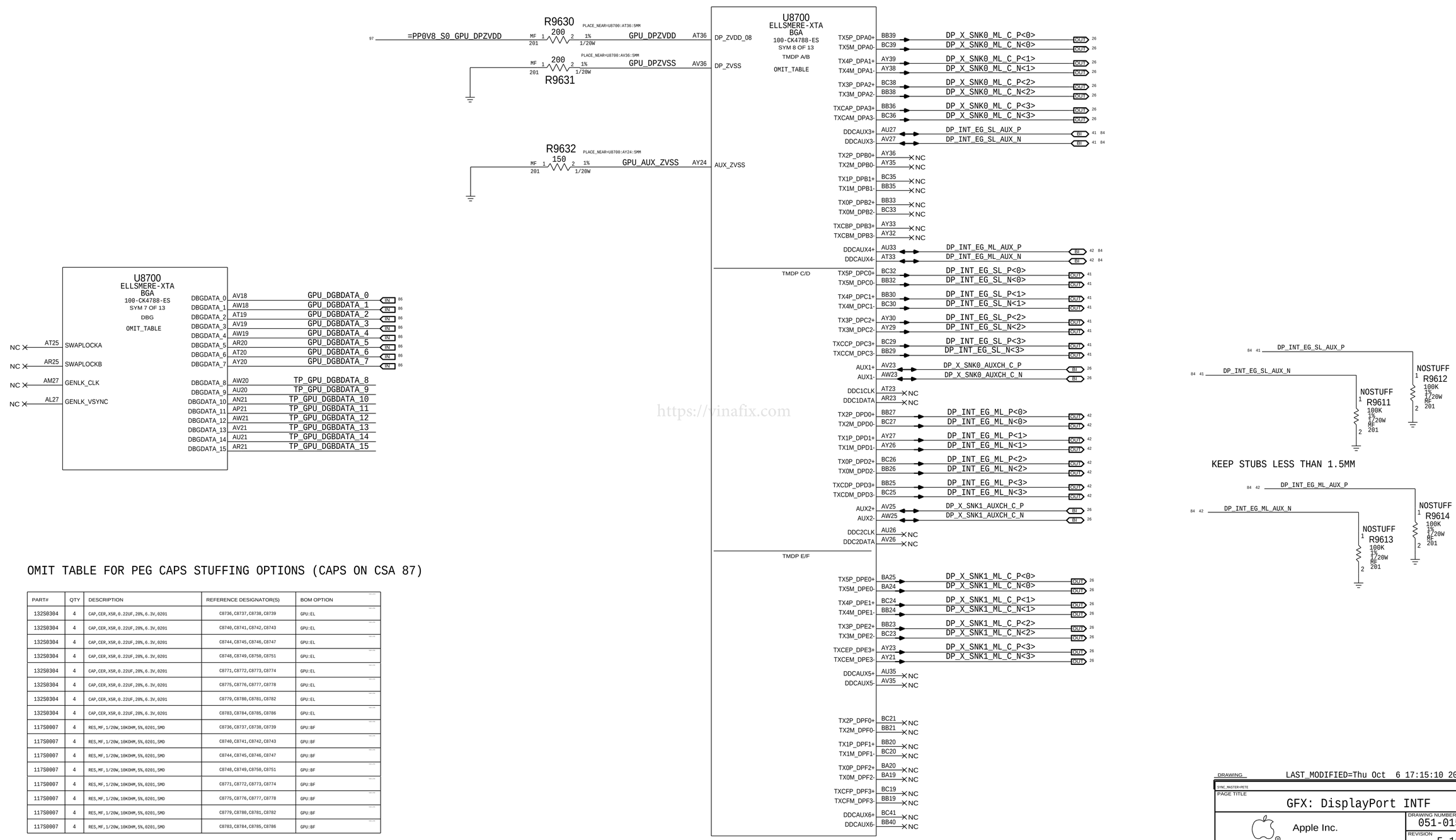

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OMIT TABLE FOR PEG CAPS STUFFING OPTIONS (CAPS ON CSA 87)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0304	4	CAP,CER,X5R,0.22UF,20%,6.3V,0201	C8736,C8737,C8738,C8739	GPU:EL
132S0304	4	CAP,CER,X5R,0.22UF,20%,6.3V,0201	C8740,C8741,C8742,C8743	GPU:EL
132S0304	4	CAP,CER,X5R,0.22UF,20%,6.3V,0201	C8744,C8745,C8746,C8747	GPU:EL
132S0304	4	CAP,CER,X5R,0.22UF,20%,6.3V,0201	C8748,C8749,C8750,C8751	GPU:EL
132S0304	4	CAP,CER,X5R,0.22UF,20%,6.3V,0201	C8771,C8772,C8773,C8774	GPU:EL
132S0304	4	CAP,CER,X5R,0.22UF,20%,6.3V,0201	C8775,C8776,C8777,C8778	GPU:EL
132S0304	4	CAP,CER,X5R,0.22UF,20%,6.3V,0201	C8779,C8780,C8781,C8782	GPU:EL
132S0304	4	CAP,CER,X5R,0.22UF,20%,6.3V,0201	C8783,C8784,C8785,C8786	GPU:EL
117S0007	4	RES,MF,1/20W,10KOHM,5%,0201,SMD	C8736,C8737,C8738,C8739	GPU:BF
117S0007	4	RES,MF,1/20W,10KOHM,5%,0201,SMD	C8740,C8741,C8742,C8743	GPU:BF
117S0007	4	RES,MF,1/20W,10KOHM,5%,0201,SMD	C8744,C8745,C8746,C8747	GPU:BF
117S0007	4	RES,MF,1/20W,10KOHM,5%,0201,SMD	C8748,C8749,C8750,C8751	GPU:BF
117S0007	4	RES,MF,1/20W,10KOHM,5%,0201,SMD	C8771,C8772,C8773,C8774	GPU:BF
117S0007	4	RES,MF,1/20W,10KOHM,5%,0201,SMD	C8775,C8776,C8777,C8778	GPU:BF
117S0007	4	RES,MF,1/20W,10KOHM,5%,0201,SMD	C8779,C8780,C8781,C8782	GPU:BF
117S0007	4	RES,MF,1/20W,10KOHM,5%,0201,SMD	C8783,C8784,C8785,C8786	GPU:BF

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SYNC_MASTER=PETE SYNC_DATE=07/17/2016

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GFX: DisplayPort INTF

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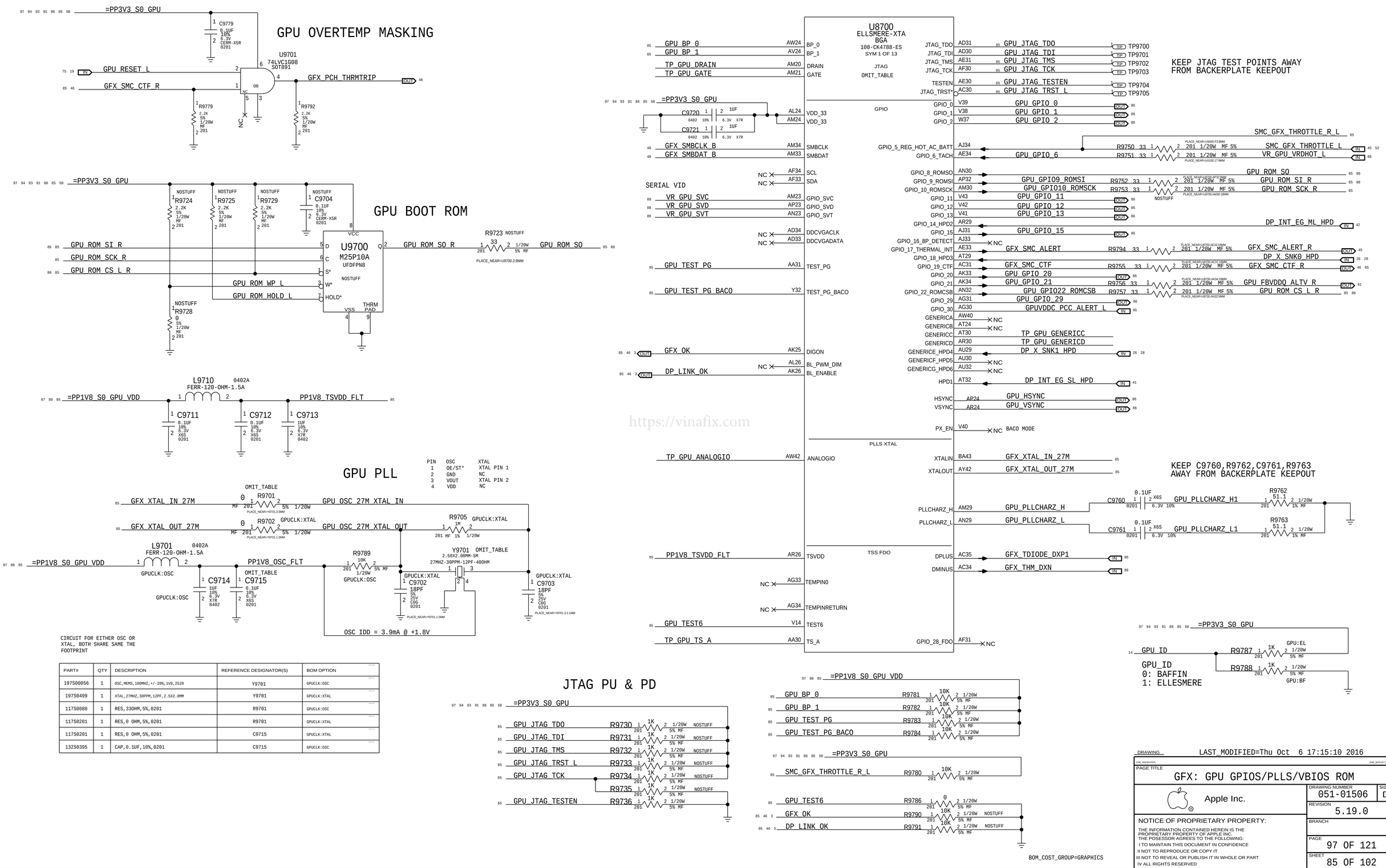
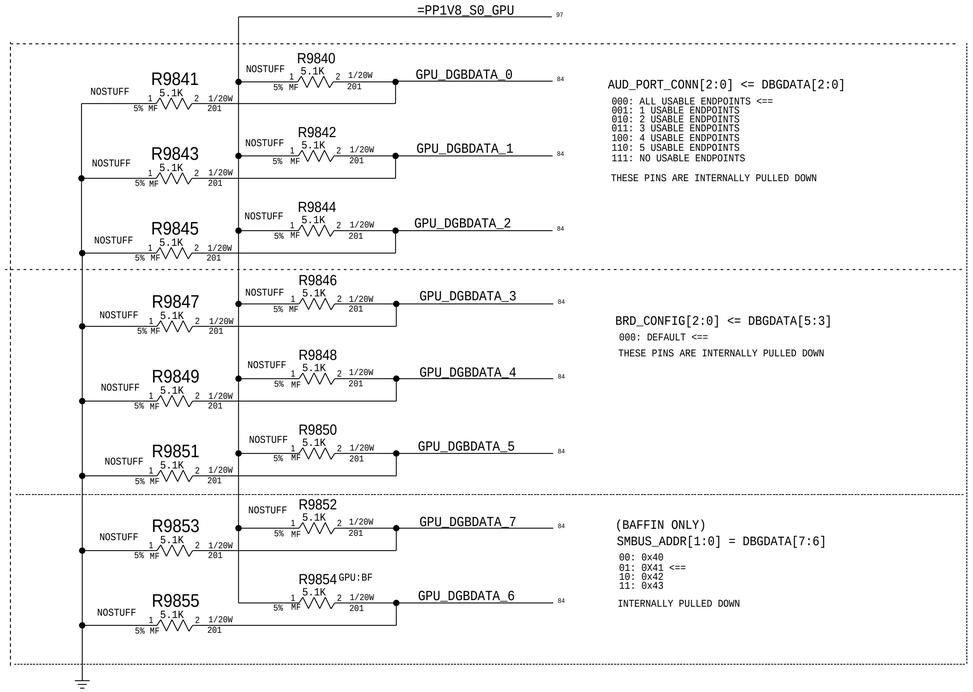


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
197S00056	1	OSC,MEMS,100MHZ,+/-20%,1V8,2520	Y9701	GPUCLK:OSC
197S0499	1	XTAL,27MHZ,30PPM,12PF,2.5X2.0MM	Y9701	GPUCLK:XTAL
117S0080	1	RES,330HM,5%,0201	R9701	GPUCLK:OSC
117S0201	1	RES,0 OHM,5%,0201	R9701	GPUCLK:XTAL
117S0201	1	RES,0 OHM,5%,0201	C9715	GPUCLK:XTAL
132S0395	1	CAP,0.1UF,10%,0201	C9715	GPUCLK:OSC

PIN-BASED CONFIG STRAPS

+1.8V PIN STRAPS



AUD_PORT_CONN[2:0] <= DBGDATA[2:0]

000: ALL USABLE ENDPOINTS <==
001: 1 USABLE ENDPOINTS
010: 2 USABLE ENDPOINTS
011: 3 USABLE ENDPOINTS
100: 4 USABLE ENDPOINTS
110: 5 USABLE ENDPOINTS
111: NO USABLE ENDPOINTS

THESE PINS ARE INTERNALLY PULLED DOWN

BRD_CONFIG[2:0] <= DBGDATA[5:3]

000: DEFAULT <==

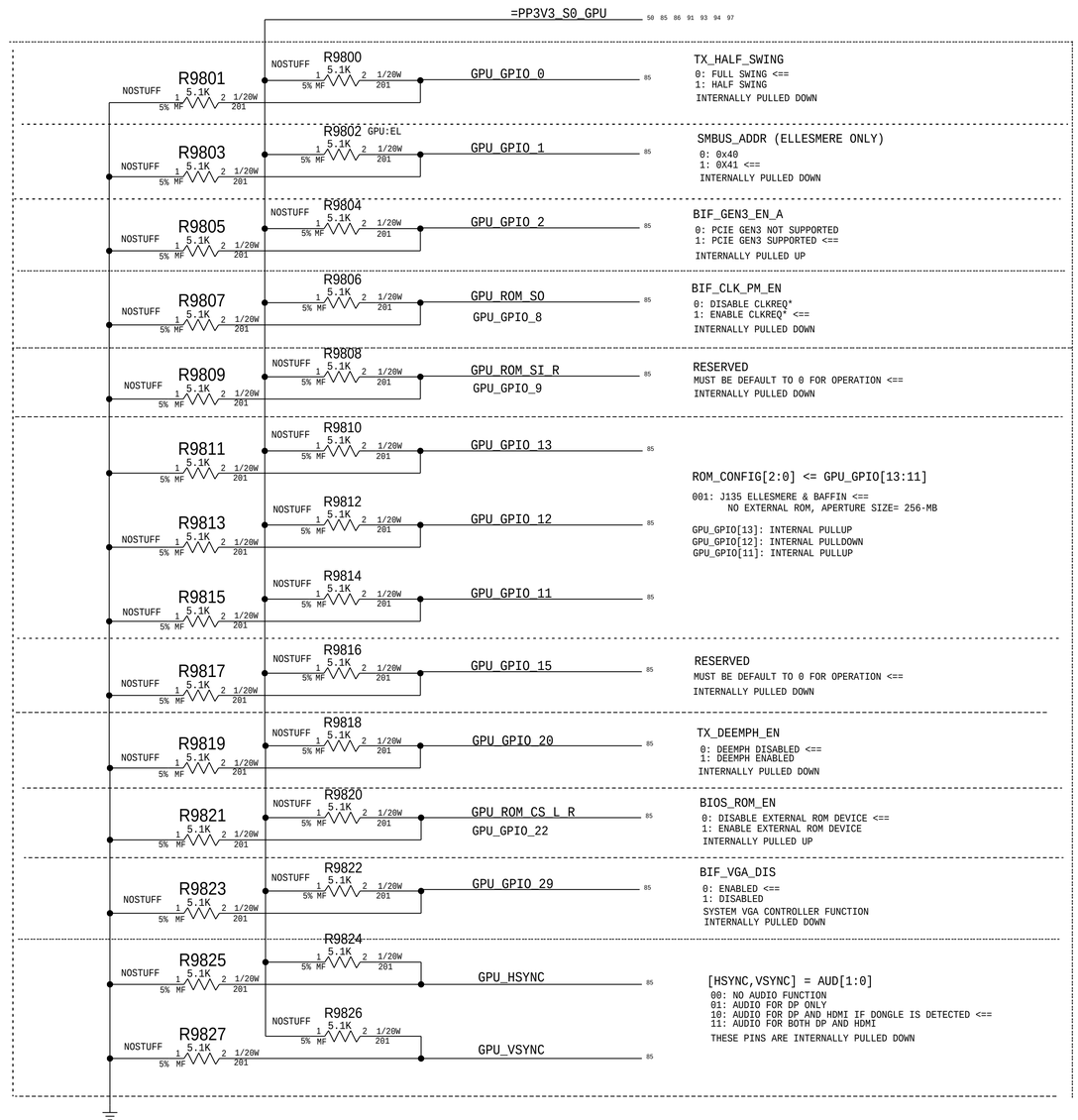
THESE PINS ARE INTERNALLY PULLED DOWN

(BAFFIN ONLY)
SMBUS_ADDR[1:0] = DBGDATA[7:6]

00: 0x40
01: 0x41 <==
10: 0x42
11: 0x43

INTERNALLY PULLED DOWN

+3.3V PIN STRAPS



TX_HALF_SWING
0: FULL SWING <==
1: HALF SWING
INTERNALLY PULLED DOWN

SMBUS_ADDR (ELLESMERE ONLY)
0: 0x40
1: 0X41 <==
INTERNALLY PULLED DOWN

BIF_GEN3_EN_A
0: PCIE GEN3 NOT SUPPORTED
1: PCIE GEN3 SUPPORTED <==
INTERNALLY PULLED UP

BIF_CLK_PM_EN
0: DISABLE CLKREQ*
1: ENABLE CLKREQ* <==
INTERNALLY PULLED DOWN

RESERVED
MUST BE DEFAULT TO 0 FOR OPERATION <==
INTERNALLY PULLED DOWN

ROM_CONFIG[2:0] <= GPU_GPIO[13:11]

001: J135 ELLESMERE & BAFFIN <==
NO EXTERNAL ROM, APERTURE SIZE= 256-MB

GPU_GPIO[13]: INTERNAL PULLUP
GPU_GPIO[12]: INTERNAL PULLDOWN
GPU_GPIO[11]: INTERNAL PULLUP

RESERVED
MUST BE DEFAULT TO 0 FOR OPERATION <==
INTERNALLY PULLED DOWN

TX_DEEMPH_EN
0: DEEMPH DISABLED <==
1: DEEMPH ENABLED
INTERNALLY PULLED DOWN

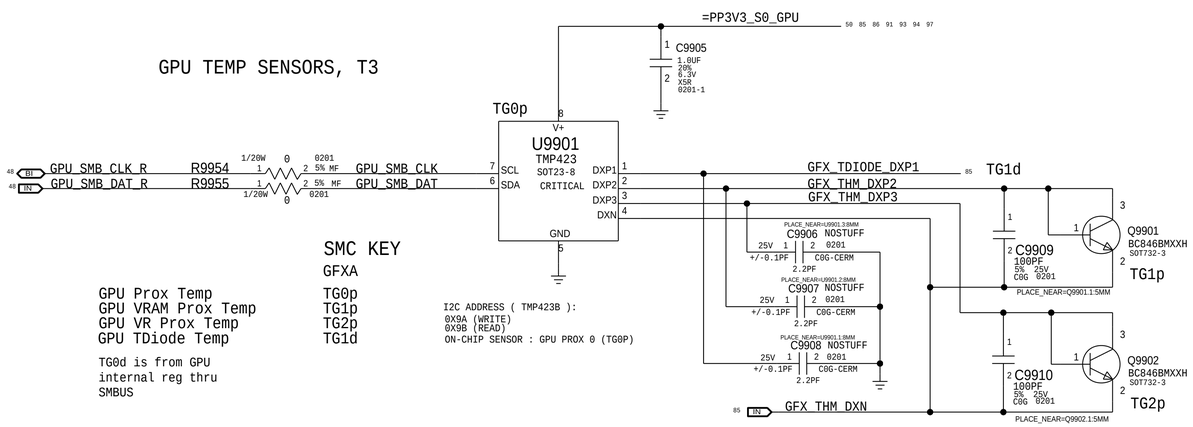
BIOS_ROM_EN
0: DISABLE EXTERNAL ROM DEVICE <==
1: ENABLE EXTERNAL ROM DEVICE
INTERNALLY PULLED UP

BIF_VGA_DIS
0: ENABLED <==
1: DISABLED
SYSTEM VGA CONTROLLER FUNCTION
INTERNALLY PULLED DOWN

[HSYNC,VSYNC] = AUD[1:0]
00: NO AUDIO FUNCTION
01: AUDIO FOR DP ONLY
10: AUDIO FOR DP AND HDMI IF DONGLE IS DETECTED <==
11: AUDIO FOR BOTH DP AND HDMI

THESE PINS ARE INTERNALLY PULLED DOWN

GPU TEMP SENSORS, T3



SMC KEY

GFXA	
GPU Prox Temp	TG0p
GPU VRAM Prox Temp	TG1p
GPU VR Prox Temp	TG2p
GPU TDiode Temp	TG1d

TG0d is from GPU
internal reg thru
SMBUS

I2C ADDRESS (TMP423B):
0X9A (WRITE)
0X9B (READ)
ON-CHIP SENSOR : GPU PROX 0 (TG0P)

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PAGE TITLE	GFX: GPU STRAPS/TEMP SENSORS
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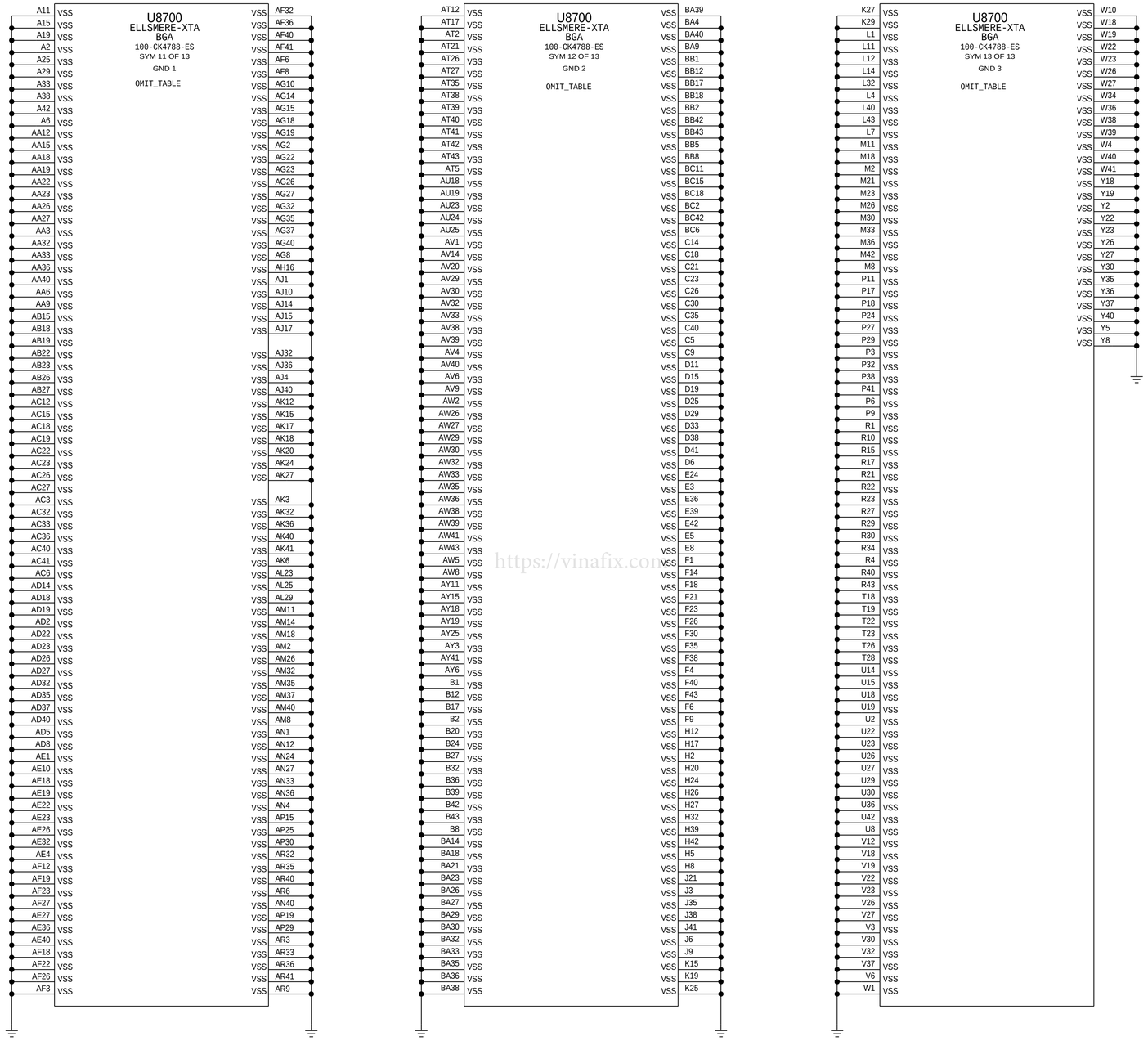

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DRAWING LAST_MODIFIED=Thu Oct 6 17:15:10 2016

PAGE TITLE
GFX: GPU GNDS

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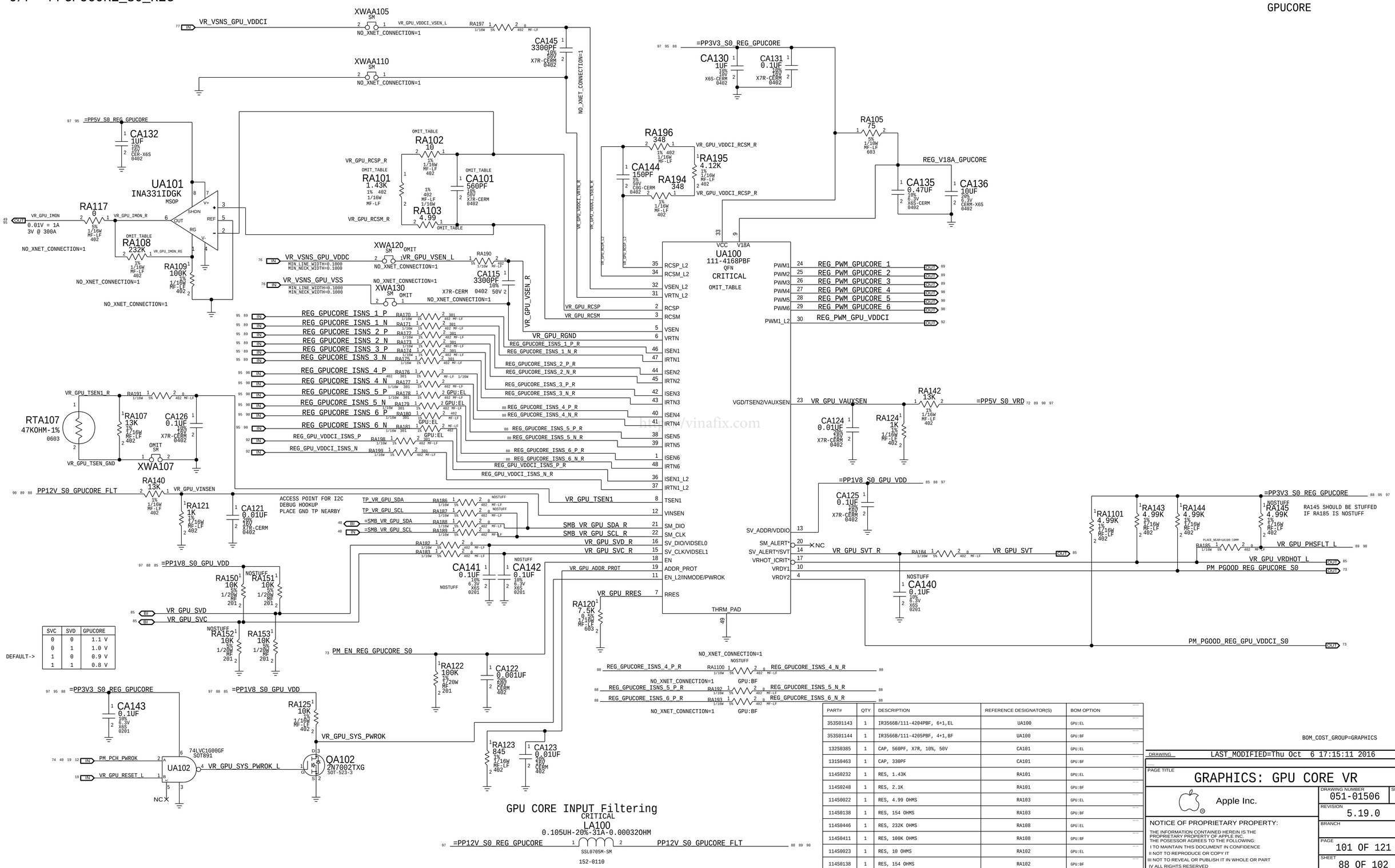
O/P= PPGPUCORE_S0_REG

GPUCORE



SVC	SVD	GPUCORE
0	0	1.1 V
0	1	1.0 V
1	0	0.9 V
1	1	0.8 V

DEFAULT->

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S01143	1	IR3566B/111-4204PBF, 6+1,EL	UA100	GPU:EL
353S01144	1	IR3566B/111-4205PBF, 4+1,BF	UA100	GPU:BF
132S0385	1	CAP, 560PF, X7R, 10%, 50V	CA101	GPU:EL
131S0463	1	CAP, 330PF	CA101	GPU:BF
114S0232	1	RES, 1.43K	RA101	GPU:EL
114S0248	1	RES, 2.1K	RA101	GPU:BF
114S0022	1	RES, 4.99 OHMS	RA103	GPU:EL
114S0138	1	RES, 154 OHMS	RA103	GPU:BF
114S0446	1	RES, 232K OHMS	RA108	GPU:EL
114S0411	1	RES, 100K OHMS	RA108	GPU:BF
114S0023	1	RES, 10 OHMS	RA102	GPU:EL
114S0138	1	RES, 154 OHMS	RA102	GPU:BF

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PAGE TITLE
GRAPHICS: GPU CORE VR

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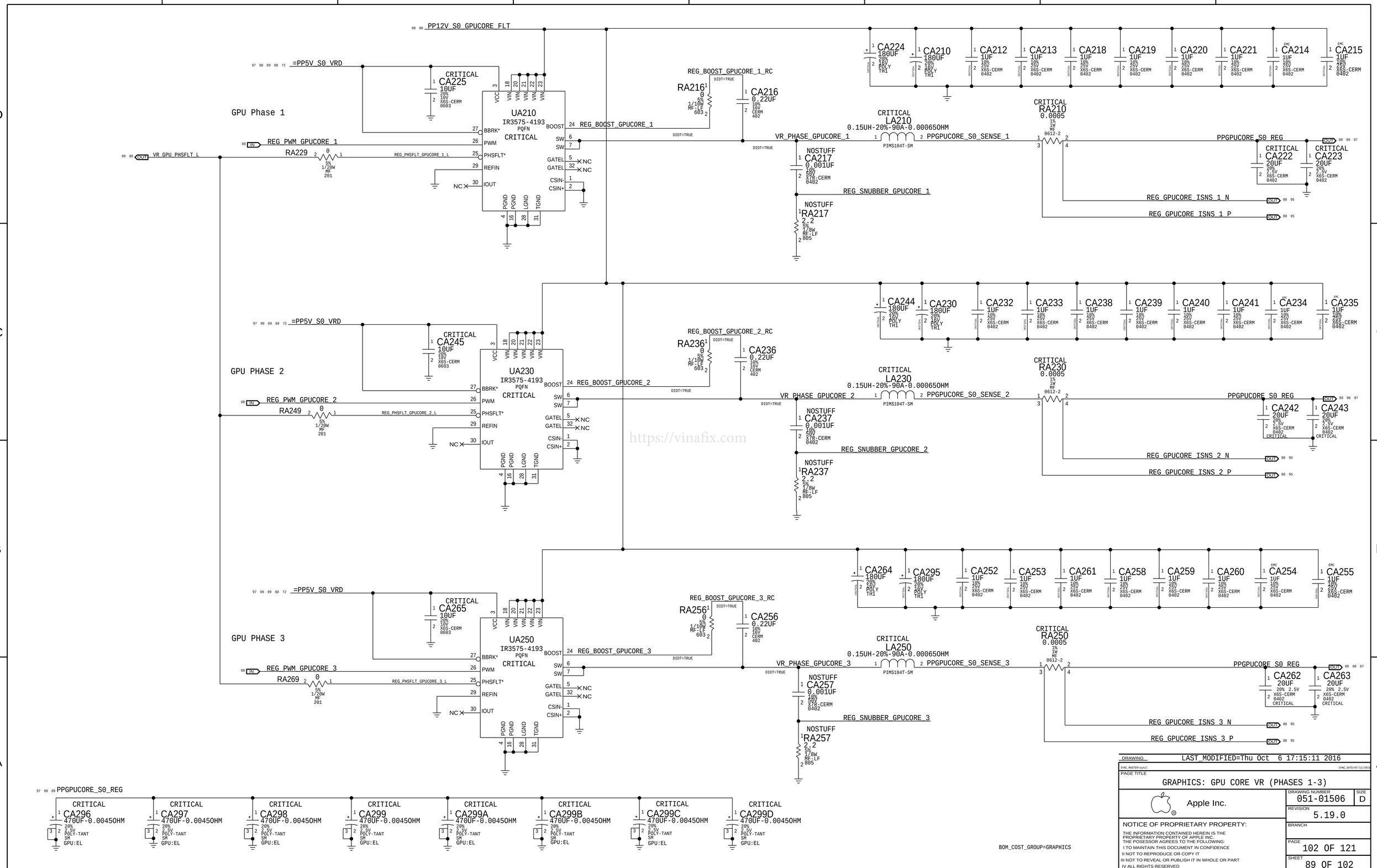

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PAGE TITLE: GRAPHICS: GPU CORE VR (PHASES 1-3)

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DRAWING NUMBER: 051-01506 SIZE: D

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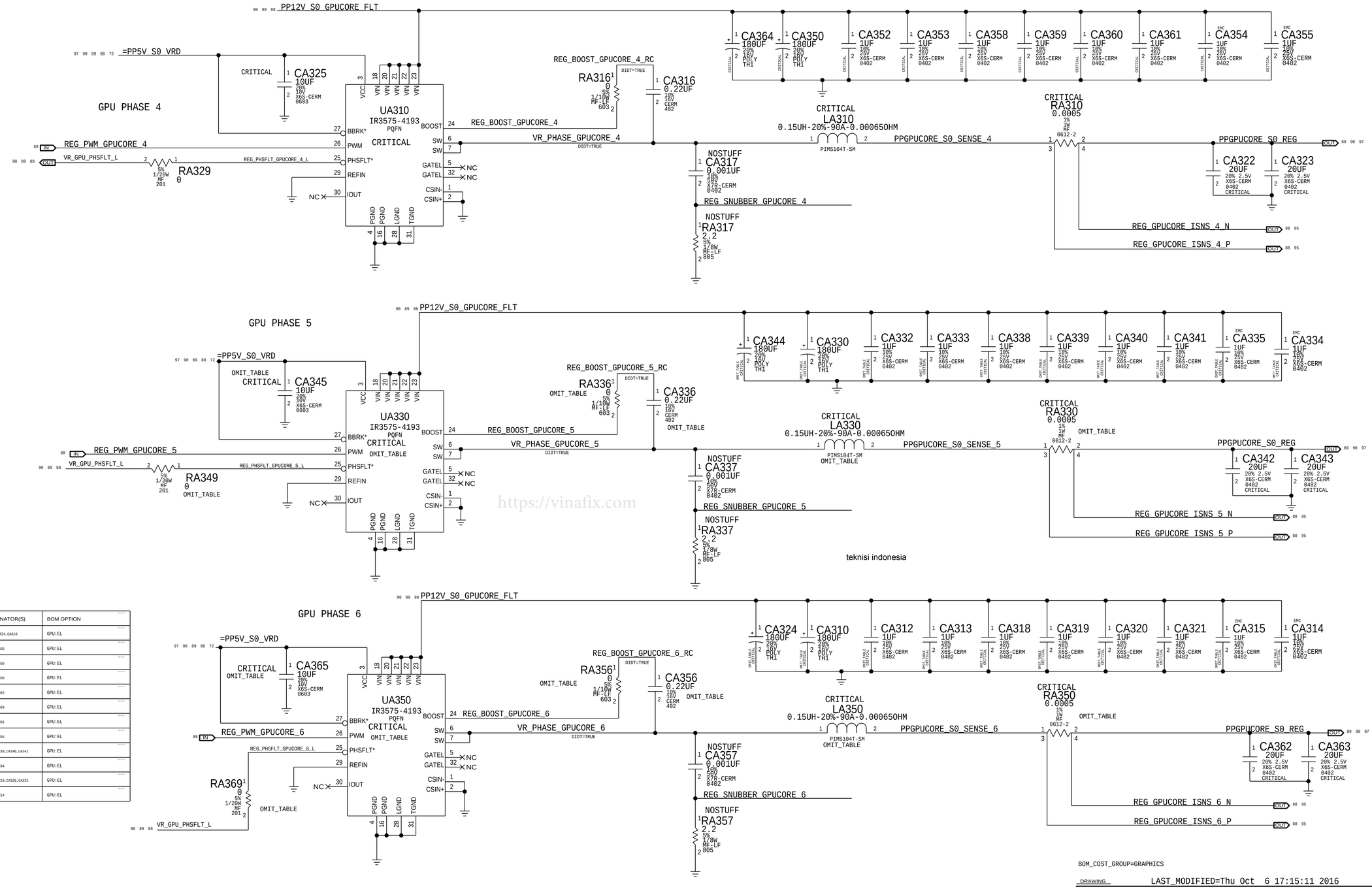

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
124-0403	4	CAP,180uF,10V, POLY, TH1	CA344,CA330,CA324,CA310	GPU:EL
107S00039	2	RES,0.0005,1%,1W,0612-2	RA330,RA350	GPU:EL
152S00302	2	IND,150nH,0.00064	LA330,LA350	GPU:EL
353S01013	2	IC,IR3575M	UA330,UA350	GPU:EL
138S0768	2	CAP,10uF,10V,X6S,0603	CA345,CA365	GPU:EL
117S0002	2	RES,0,5%,201	RA349,RA369	GPU:EL
113S0022	2	RES,0,5%,603	RA336,RA356	GPU:EL
132S0301	2	CAP,0.22uF,10V,402	CA336,CA356	GPU:EL
138S0775	6	CAP,1uF,25V,X6S,402	CA332,CA333,CA338,CA339,CA340,CA341	GPU:EL
138S0775	2	CAP,1uF,25V,X6S,402	CA335,CA334	GPU:EL
138S0775	6	CAP,1uF,25V,X6S,402	CA312,CA313,CA318,CA319,CA320,CA321	GPU:EL
138S0775	2	CAP,1uF,25V,X6S,402	CA315,CA314	GPU:EL

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PAGE TITLE
GRAPHICS: GPU CORE VR (PHASES 4-6)

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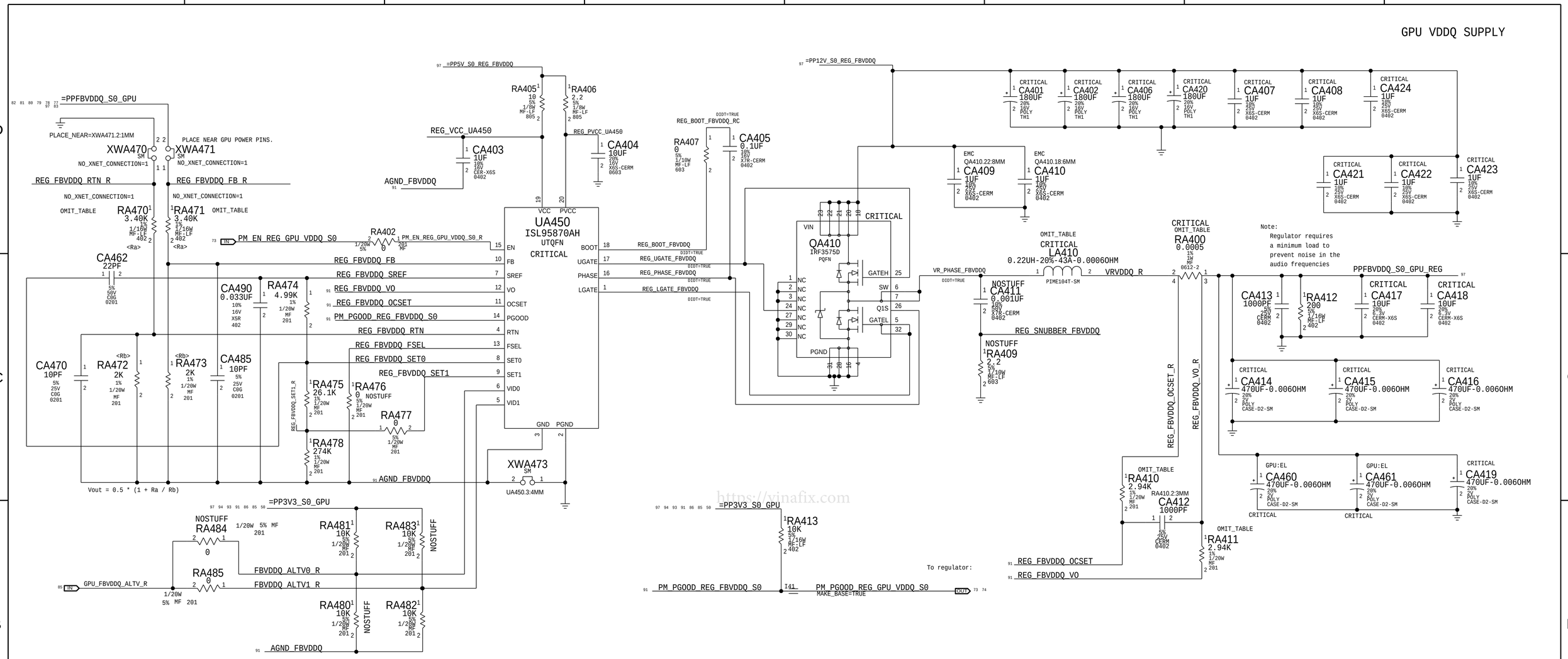

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VID 1	VID 0	GPU VDDQ
1	1	1.35 V
DEFAULT -> 0	1	1.5 V

GPU VDDQ	RA470 = RA471
1.5 V	3.4K
1.55 V	3.57K
1.6 V	3.74K

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
152S00176	1	IND,0.22UH,43A,0.64mOHM	LA410	GPU:EL
152S1799	1	IND,0.36UH,40A,0.8mOHM	LA410	GPU:BF
107S00039	1	RES,0.0005OHM,1%,0612-4T	RA400	GPU:EL
107S0255	1	RES,0.001OHM,1%,0612-4T	RA400	GPU:BF
114S0269	2	RES,3.4K,1%,0402	RA470, RA471	VR_VRAM_HYN_1V50
114S0271	2	RES,3.57K,1%,0402	RA470, RA471	VR_VRAM_HYN_1V55
114S0269	2	RES,3.4K,1%,0402	RA470, RA471	VR_VRAM_SAM_1V50
114S0271	2	RES,3.57K,1%,0402	RA470, RA471	VR_VRAM_SAM_1V55
114S0271	2	RES,3.57K,1%,0402	RA470, RA471	VR_VRAM_ELP_1V55
114S0273	2	RES,3.74K,1%,0402	RA470, RA471	VR_VRAM_SAM_1V60
114S0273	2	RES,3.74K,1%,0402	RA470, RA471	VR_VRAM_ELP_1V60
118S0269	2	RES,2.94K	RA410, RA411	GPU:EL
118S0269	2	RES,2.94K	RA410, RA411	GPU:BF
114S0269	2	RES,3.4K	RA470, RA471	VR_VRAM_ELP_1V50

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PAGE TITLE
GRAPHICS: GPU VDDQ VR

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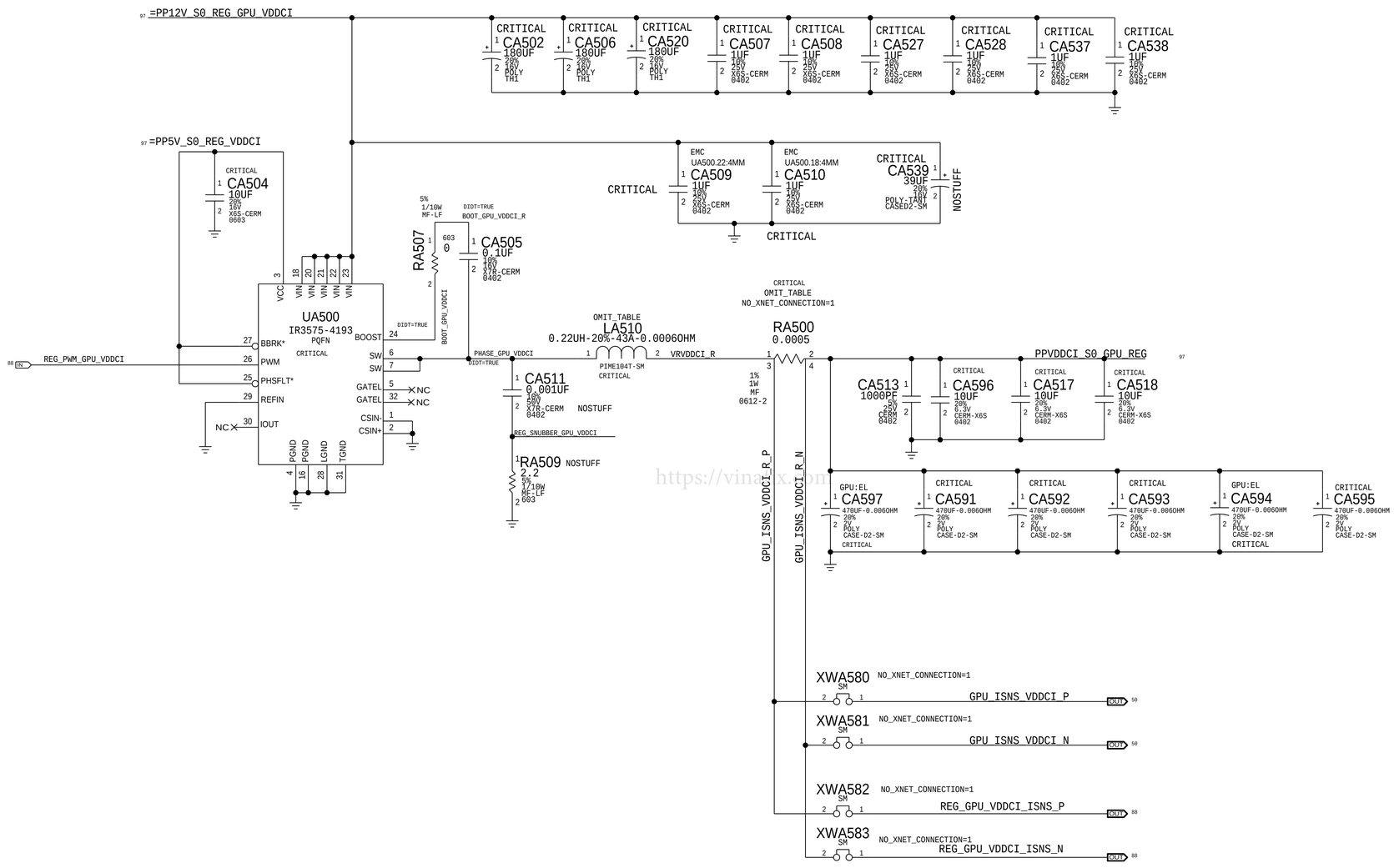
GPU VDDCI SUPPLY



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
152S00176	1	IND,0.22UH,43A,0.64mOHM	LA510	GPU:EL
152S1799	1	IND,0.36UH,40A,0.8mOHM	LA510	GPU:BF
107S00039	1	RES,0.0005OHM,1%,0612-4T	RA500	GPU:EL
107S0255	1	RES,0.001OHM,1%,0612-4T	RA500	GPU:BF

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PAGE TITLE
GRAPHICS: GPU VDDCI VR

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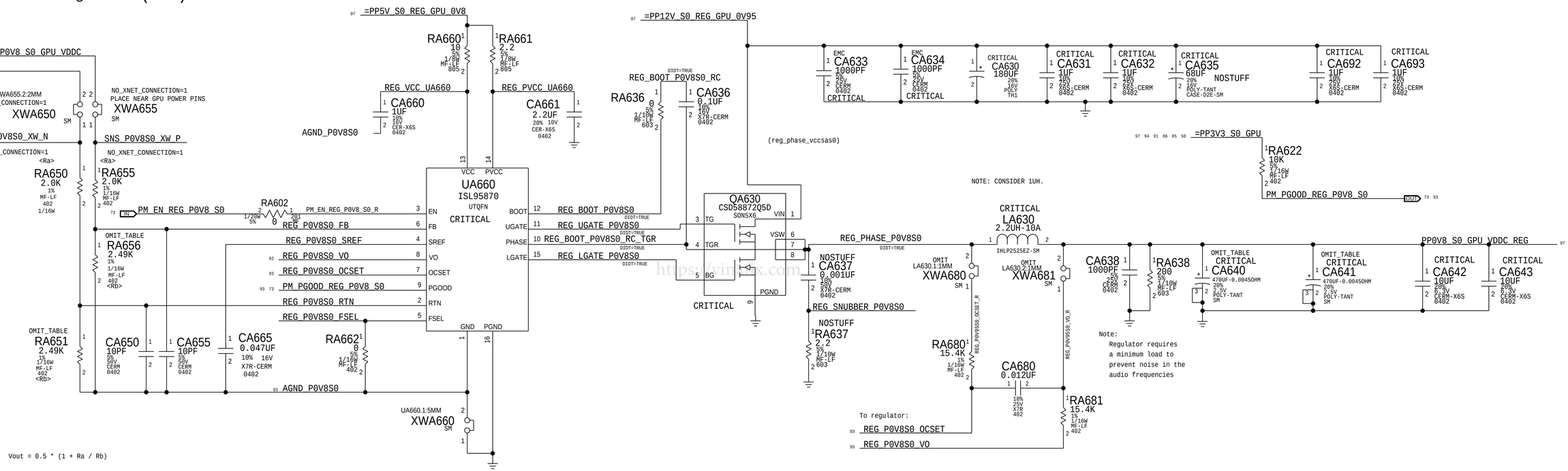
GPU VDDC (0.8V) S0 REGULATOR

GPU VDDC = 0.8V @ 4.6A (EDP)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
128S0358	2	CAP,470uF,0.006OHM,2V,D2	CA640,CA641	VR_BULKCAP:CURRENT
128S0381	2	CAP,470uF,0.0045OHM,2.5V,SM	CA640,CA641	VR_BULKCAP:FUTURE
114S0256	2	RES, 2.49K	RA651, RA656	GPU:EL
114S0262	2	RES, 2.87K	RA651, RA656	GPU:BF

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GRAPHICS: GPU 0V8 VR

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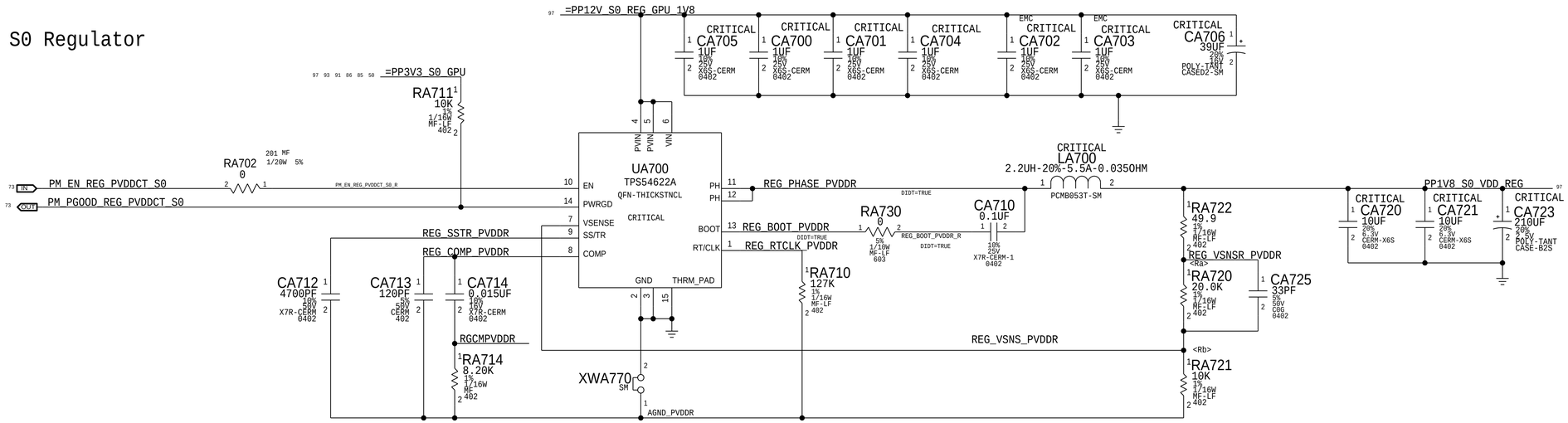
1.8V S0 Regulator



VOUT = 0.6 * (1 + RA / RB)

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SYNC_MASTER=SUNZL SYNC_DATE=07/14/2016

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GRAPHICS: GPU 1V8 VR

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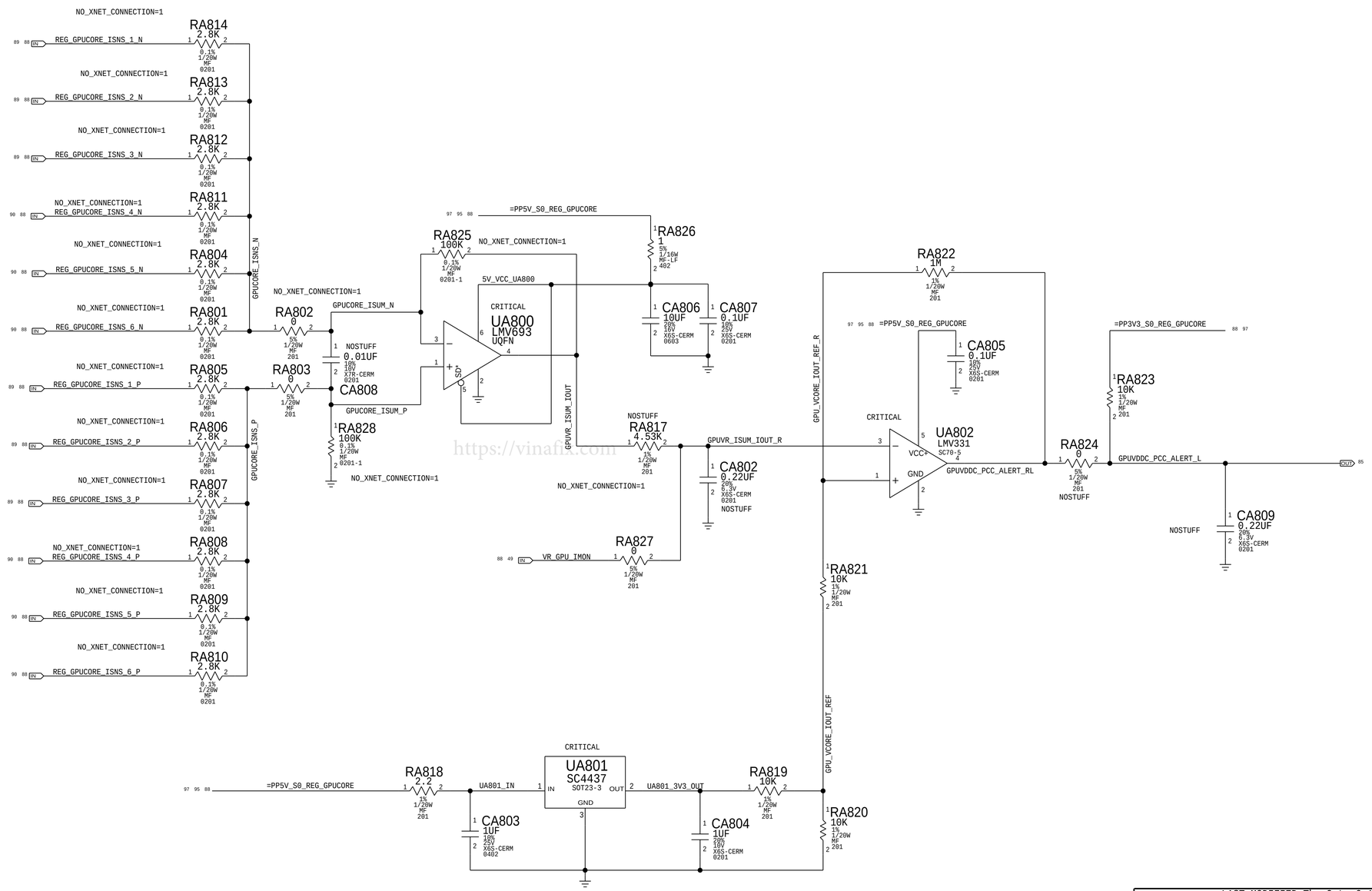

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SYNC_MASTER=sunil SYNC_DATE=01/13/2016

PAGE TITLE

GRAPHICS: GPU VR MISC

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G3 Rails
Always on: Keeps the PCH RTC alive

PP3V3_G3 (MAKE_BASE=TRUE)	PP3V3_G3_RTC	18
	=PP3V3_G3_PCH_RTC	12 15

G3H Rails
On with AC/DC plugged in

PP12V_ACDC (MAKE_BASE=TRUE)	PP12V_G3H_ACDC	61
	=PP12V_G3H_SNS_R	49
PP12V_G3H (MAKE_BASE=TRUE)	PP12V_G3H_SNS	49
	=PP12V_G3H_P3V3	61
	=PP12V_G3H_FET_P12V_S0	72
	=PP12V_G3H_FET_P12V_S5	72
PP3V3_G3H (MAKE_BASE=TRUE)	PP3V3_G3H_REG	61
	=PP3V3_G3H_BT	33
	=PP3V3_G3H_RTC_D	18
	=PP3V3_G3H_SMC	45 46 53
	=PP3V3_G3H_SMC_USBMUX	43
	=PP3V3_G3H_T112	47
	=PP3V3_G3H_LED	3
	=PP3V3_G3H_UPC_XA	29
	=PP3V3_G3H_UPC_XB	30
	=PP3V3_G3H_SMB	48
	=PP3V3_G3H_PWRCTL	73

Ground/Common

GND (MAKE_BASE=TRUE)	

S5 Rails
On when in S5

PP12V_S5 (MAKE_BASE=TRUE)	PP12V_S5_FET	72
	=PP12V_S5_FET_P3V3_S5_P5V_S4	67
	=PP12V_S5_REG_VDDQ_S3	65
	=PP12V_S5_PWRCTL	73
	=PPHV_SW_TBT_X	28
	=PP12V_S5_SNS	49
	=PP12V_S5_REG_P1V0_S5	68
PP5V_S5 (MAKE_BASE=TRUE)	PP5V_S5_LDO	67
	=PP5V_S5_REG_P1V0	68
	=PP5V_S5_PCC	52
PP3V3_S5_SNS (MAKE_BASE=TRUE)	PP3V3_S5_REG	67
	=PP3V3_S5_REG_SNS_R	50
PP3V3_S5 (MAKE_BASE=TRUE)	PP3V3_S5_REG_SNS	50
	=PP3V3_S5_FET_P3V3_S0	72
	=PP3V3_S5_FET_P3V3_S4	72
	=PP3V3_S5_SMC	34 46
	=PP3V3_S5_PCH_VCC	12 13 14 15 19
	=PP3V3_S5_PWRCTL	34 72 73 74
	=PP3V3_S5_ROM	17 47
	=PP3V3_S5_VRD	67 68
	=PP3V3_S5_SENSE	49 52
	=PP3V3_S5_RSTBUF	19
	=PP3V3_S5_LDO_P1V8_S5	68
	=PP3V3_S5_SSD	34
	=PP3V3_S5_REG_P2V5_S3	65
PP1V8_S5 (MAKE_BASE=TRUE)	PP1V8_S5_LDO	68
	=PP1V8_S5_PCH_VCCHDA	15 18
	=PP1V8_S5_PWRCTL	73
PP1V0_S5 (MAKE_BASE=TRUE)	PP1V0_S5_REG	68
	=PP1V0_S5_PCH_VCC	11 15
	=PP1V0_S5_XDP	17
	=PP1V0_S5_FET_PP1V0_S3	72

S4 Rails
Enabled when system has AC and is in run or sleep

PP5V_S4_SNS (MAKE_BASE=TRUE)	PP5V_S4_REG	67
	=PP5V_S4_REG_SNS_R	50
PP5V_S4 (MAKE_BASE=TRUE)	PP5V_S4_REG_SNS	50
	=PP5V_S4_REG_VDDQ_S3	65
	=PP5V_S4_FET_P5V_S0	72
	=PP5V_S4_CPUCOREVR	62
	=PP5V_S4_USB	43 44
	=PP5V_S4_USBC	28
	=PP5V_S4_PWRCTL	72
PP3V3_S4 (MAKE_BASE=TRUE)	PP3V3_S4_FET	72
	=PP3V3_S4_FET_ENET	37
	=PP3V3_S4_PWRCTL	65 72
	=PP3V3_S4_LED	3
	=PP3V3_S4_MEMRESET	6
	=PP3V3_S4_PCH_VCC	12 13 14
	=PP3V3_S4_SDCARD	38
	=PP3V3_S4_SMC	46
	=PP3V3_S4_TBT	19
	=PP3V3_UPC_XA_AUX	29
	=PP3V3_UPC_XB_AUX	30
	=PP3V3_S4_AP	33 46
97 34 PP3V3_S4_FET_SSD (MAKE_BASE=TRUE)	PP3V3_S4_FET_SSD	34 97
	=PPVSSD_S4_REG_SNS_R	50
PP3V3_S4_SSD (MAKE_BASE=TRUE)	PPVSSD_S4_REG_SNS	50
	=PP3V3_S4_SSD_CONN	34

S3 Rails
Enabled when system is in run or sleep

PP3V3_ENET (MAKE_BASE=TRUE)	PP3V3_ENET_FET	37
	=PP3V3_ENET_PHY	36 37
PPVDDQ_S3 (MAKE_BASE=TRUE)	PPVDDQ_S3_REG	65
	=PPVDDQ_S3_SNS_DDR_R	50
THIS IS 1.2V RAIL	=PP1V2_S3_SNS_R	50
PPVDDQ_S3_DDR (MAKE_BASE=TRUE)	PPVDDQ_S3_SNS_DDR	50
	=PPDDR_S3_MEMVREF	20
THIS IS 1.2V RAIL	=PPVDDQ_S3_MEM_A	21 22
	=PPVDDQ_S3_MEM_B	23 24
	=PPVDDQ_S3_MEMRESET	12
	=PPVDDQ_S3_LDO_DDRVTT	65
PP1V2_S3_CPU (MAKE_BASE=TRUE)	PP1V2_S3_SNS	50
	=PPVDDQ_S3_CPU	8 10
PP1V0_S3_CPU_VCCST (MAKE_BASE=TRUE)	PP1V0_S3_FET	72
	=PP1V0_S3_VCCST	12 62
	=PP1V0_S3_SMC	46
	=PP1V0_S3_XDP	17
	=PP1V0_S3_CPU	6 8 10
PP2V5_S3 (MAKE_BASE=TRUE)	PP2V5_S3_REG	65
	=PPDDRVPP_S3_MEM_A	21 22
	=PPDDRVPP_S3_MEM_B	23 24

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S0 Rails
Enabled when system is in run

PP12V_S0 (MAKE_BASE=TRUE)	PP12V_S0_FET	72
	=PP12V_S0_AUDIO_SPKRAMP	56 57
	=PP12V_S0_FAN	53
	=PP12V_S0_SNS_GPUCORE_R	49
	=PP12V_S0_LCD	41
	=PP12V_S0_CPUCORE	62
	=PP12V_S0_SNS_FBVDDQ_R	49
	=PP12V_S0_HDD	35
	=PP12V_S0_BKLT	70
PP12V_S0_GPU_AUX (MAKE_BASE=TRUE)	PP12V_S0_SNS_GPU_AUX	49
	=PP12V_S0_REG_GPU_0V95	93
	=PP12V_S0_REG_GPU_1V8	94
PP12V_S0_GPUCORE (MAKE_BASE=TRUE)	PP12V_S0_SNS_GPUCORE	49
	=PP12V_S0_REG_GPUCORE	88
	=PP12V_S0_REG_GPU_VDDCI	92
97 62 PP12V_S0_CPUCORE_FLT (MAKE_BASE=TRUE)	PP12V_S0_CPUCORE_FLT	62 97
	=PP12V_S0_SNS_CPUCORE_R	49
PP12V_S0_CPUCORE (MAKE_BASE=TRUE)	PP12V_S0_SNS_CPUCORE	49
	=PP12V_S0_REG_CPUCORE	62 63 64 66 69
PPHDD12_S0 (MAKE_BASE=TRUE)	PP12V_S0_HDD_FET	35
	=PP12V_S0_HDD_SNS_R	50
PP12V_S0_HDD (MAKE_BASE=TRUE)	PP12V_S0_HDD_SNS	50
	=PP12V_S0_HDD_PWR	35
PP12V_S0_FBVDDQ (MAKE_BASE=TRUE)	PP12V_S0_SNS_FBVDDQ	49
	=PP12V_S0_REG_FBVDDQ	91
PP5V_S0 (MAKE_BASE=TRUE)	PP5V_S0_FET	72
	=PP5V_S0_BKLT	70
	=PP5V_S0_ISENSE	49
	=PP5V_S0_REG_CPUVCC_S0	63 64 66 69
	=PP5V_S0_REG_FBVDDQ	91
	=PP5V_S0_HDD	35
	=PP5V_S0_VRD	72 88 89 90
	=PP5V_S0_REG_VDDCI	92
	=PP5V_S0_REG_GPU_0V8	93
	=PP5V_S0_CAMERA	39
	=PP5V_S0_REG_GPUCORE	88 95
PPHDD_S0 (MAKE_BASE=TRUE)	PP5V_S0_HDD_FET	35
	=PPHDD_S0_SNS_R	50
PP5V_S0_HDD (MAKE_BASE=TRUE)	PPHDD_S0_SNS	50
	=PP5V_S0_HDD_PWR	35
PP3V3_S0 (MAKE_BASE=TRUE)	PP3V3_S0_FET	72
	=PP3V3_S0_AUDIO	55 58
	=PP3V3_S0_BKLT	70
	=PP3V3_S0_DP	41
	=PP3V3_S0_ENET	36
	=PP3V3_S0_FAN	53
	=PP3V3_S0_GPU	50 85 86 91 93 94
	=PP3V3_S0_INTDPMUX	41 42
	=PP3V3_S0_LED	3
	=PP3V3_S0_LED_SATA	35
	=PP3V3_S0_MEM_A_SPD	21 22
	=PP3V3_S0_MEM_B_SPD	23 24
	=PP3V3_S0_PCH_VCC	11 12 14 15 18
	=PP3V3_S0_PWRCTL	72
	=PP3V3_S0_RSTBUF	19
	=PP3V3_S0_SDCARD	38
	=PP3V3_S0_SENSE	35 49 50 51
	=PP3V3_S0_SMBUS	48
	=PP3V3_S0_SMBUS_SMC_0	48
	=PP3V3_S0_SMBUS_SMC_1	48
	=PP3V3_S0_SMBUS_SMC_3	48
	=PP3V3_S0_SMC	46
	=PP3V3_S0_VRD	61 62 66
	=PP3V3_S0_CAMERA	39 48
	=PP3V3_S0_ALS	39
	=PP3V3_S0_SMBUS_SMC_2	48
	=PP3V3_S0_REG_GPUCORE	88 95
	=PP3V3_TBT_X_S0_R	28
PPDDRVTT_S0 (MAKE_BASE=TRUE)	PPDDRVTT_S0_LDO	65
	=PPDDRVTT_S0_MEM_A	21 22
	=PPDDRVTT_S0_MEM_B	23 24

GPU Rails (S0)
Enabled when system is in run

PPGPUCORE_S0 (MAKE_BASE=TRUE)	PPGPUCORE_S0_REG	89 90
	=PPGPUCORE_S0	76
	=PPGPUCORE_S0_SNS	49
FBVDDQ IS 1.5V		
PPFBVDDQ_S0_GPU (MAKE_BASE=TRUE)	PPFBVDDQ_S0_GPU_REG	91
	=PPFBVDDQ_S0_GPU	77 78 79 80 81 82 83 91
PPVDDCI_S0_GPU (MAKE_BASE=TRUE)	PPVDDCI_S0_GPU_REG	92
	=PPVDDCI_S0_GPU	77
PP0V8_S0_GPU_VDDC (MAKE_BASE=TRUE)	PP0V8_S0_GPU_VDDC_REG	93
	=PP0V8_S0_GPU_VDDC	93
	=PP0V8_S0_GPU_PCIEVDDC	75
	=PP0V8_S0_GPU_DPZVDD	84
PP1V8_S0_MISC (MAKE_BASE=TRUE)	PP1V8_S0_VDD_REG	94
	=PP1V8_S0_AUD_DIG_TOP	39 54 56
	=PP1V8_S0_AUD_DIG_BOT	54 55 57 58
	=PP1V8_S0_CAMERA	39 40
	=PP1V8_S0_DP	42
	=PP1V8_S0_GPU_VDD	85 88
	=PP1V8_S0_GPU_PEX_IO	75
	=PP1V8_S0_GPU	86

CPU/PCH Rails (S0)
Enabled when system is in run

PPVCC_S0_CPU (MAKE_BASE=TRUE)	PPVCC_S0_CPU_REG	63
	=PPVCC_S0_CPU	8 10
	=PPVCC_S0_SNS_CPU	49
PPVCCGT_S0_CPU (MAKE_BASE=TRUE)	PPVCCGT_S0_CPU_REG	64
	=PPVCCGT_S0_CPU	8 10
	=PPVCCGT_S0_SNS_CPU	49
PPVCCSA_S0_CPU (MAKE_BASE=TRUE)	PPVCCSA_S0_CPU_REG	69
	=PPVCCSA_S0_CPU	8 10
PPVCCIO_S0 (MAKE_BASE=TRUE)	PPVCCIO_S0_CPU_REG	66
	=PPVCCIO_S0_SNS_CPU_R	49
PPVCCIO_S0_CPU (MAKE_BASE=TRUE)	PPVCCIO_S0_SNS_CPU	49
	=PPVCCIO_S0_CPU	5 8 10 17

SYNC_MASTER=sunil SYNC_DATE=11/06/2015

PAGE TITLE
Power Connectors/Aliases

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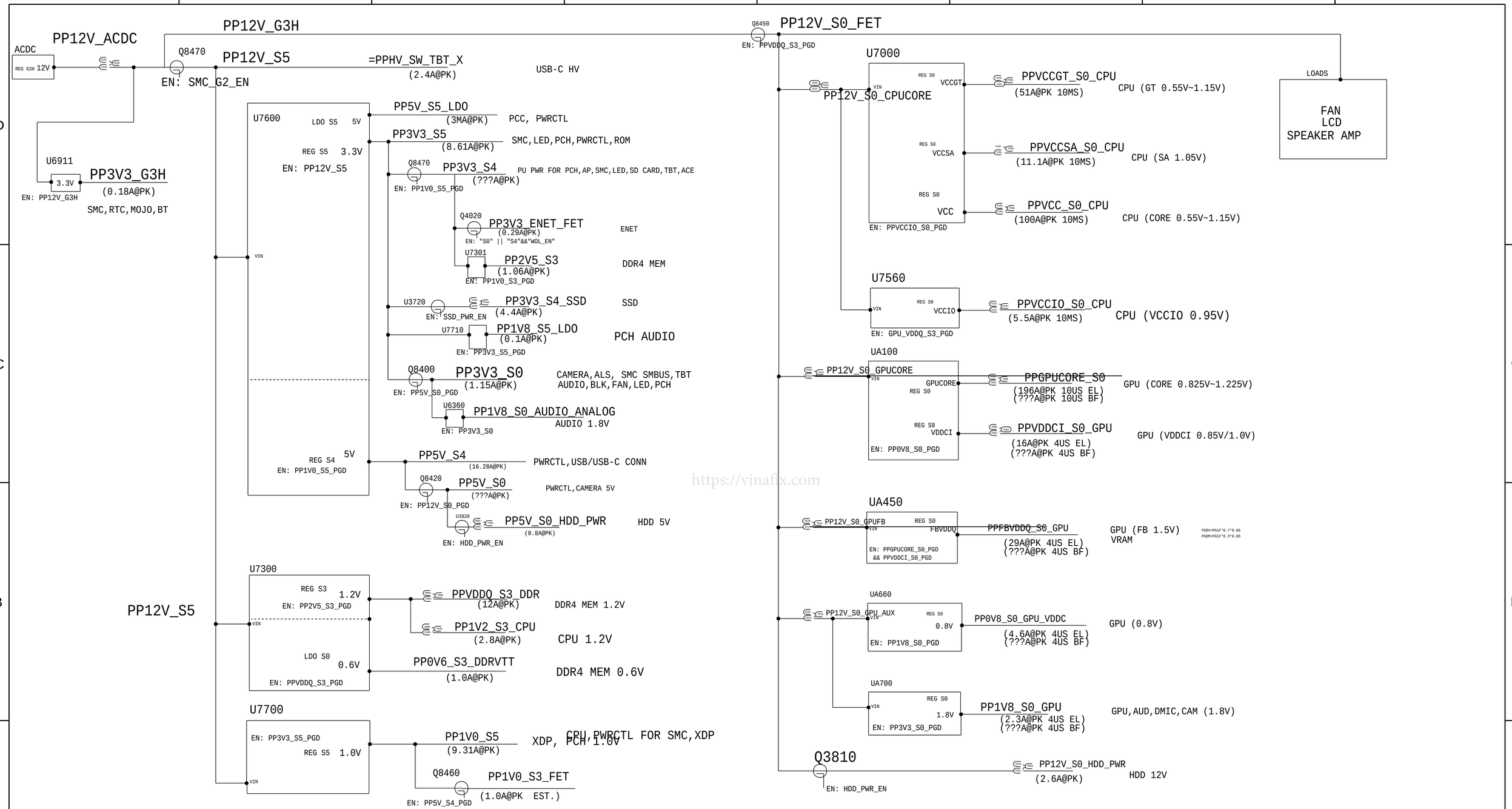

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POWER BLOCK DIAGRAM

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PEG aliases

75	PEG_D2R_N<0..15>	MAKE_BASE=TRUE	=PEG_D2R_N<15..0>	5
75	PEG_D2R_P<0..15>	MAKE_BASE=TRUE	=PEG_D2R_P<15..0>	5
75	PEG_R2D_C_N<0..15>	MAKE_BASE=TRUE	=PEG_R2D_C_N<15..0>	5
75	PEG_R2D_C_P<0..15>	MAKE_BASE=TRUE	=PEG_R2D_C_P<15..0>	5

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Signal Aliases

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CPU Reserved

17 6 CPU_CFG<15..12> — TP_CPU_CFG<15..12>
MAKE_BASE=TRUE

12 TP_CLINK_DATA — CLINK_DATA
MAKE_BASE=TRUE NO_TEST=1

12 TP_CLINK_CLK — CLINK_CLK
MAKE_BASE=TRUE NO_TEST=1

12 TP_CLINK_RESET_L — CLINK_RESAT_L
MAKE_BASE=TRUE NO_TEST=1

12 TP_PCH_SLP_LAN_L — PCH_SLP_LAN_L
MAKE_BASE=TRUE NO_TEST=1

11 TP_PCH_2 — PCH_2
MAKE_BASE=TRUE NO_TEST=1

12 TP_PM_SLP_A_L — PM_SLP_A_L
MAKE_BASE=TRUE

PCH Clocks

TP_ITPXDP_CLK100MP — ITPXDP_CLK100M_P 11 17
MAKE_BASE=TRUE

TP_ITPXDP_CLK100MN — ITPXDP_CLK100M_N 11 17
MAKE_BASE=TRUE

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PAGE TITLE
Unused Signal Aliases

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J135 ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
377S0147	377S0126		ALL	USB Diode Array	=> USB-A
197S0481	197S0480		ALL	25MHX PCH XTAL	=> ETHERNET
197S0479	197S0478		ALL	12MHZ CAM/NXP XTAL	=> CAMERA,SMC
372S0186	372S0185		ALL	Alternate Temp Diode	=> SENSOR(TEMP)
107S00030	107S00029		ALL	Alt 5mOhm sense	=> SENSORS(V/I)
341S00016	341S3912		U3990	IC,ENETROM,ADESTO,V1,15,J78	=> ETHERNET
138S0681	138S0638		ALL	10uF Caps	=> AUDIO
138S0860	138S0775		ALL	Single-source 1uF 402	=> CPU&CHIPSET,USBC, PLATFORM POWER,GRAPHICS
378S0391	378S0390		ALL	DEGUG LEDS	=> CPU&CHIPSET(LED)
311S00008	311S0271		ALL	AND GATE	=> GRAPHICS(GPU)
155S0830	155S0316		ALL	FERR BD,600 OHM,2S,0.5A	=> ETHERNET
376S00016	376S0644		ALL	MOSFET,P-CH,20V,1A	=> CPU&CHIPSET(RTC)
376S00001	376S0659		ALL	MOSFET,P-CH,20V	=> CPU&CHIPSET(RTC)
376S00015	376S0610		ALL	XSTR,FET,DL NCH,60V	=> CPU&CHIPSET(LED), ETHERNET
311S00004	311S0370		ALL	Config. Logic Gate	=> CPU&CHIPSET(ROM)
132S0447	132S0448		ALL	0.1uF 0201	=> GRAPHICS (GPU)
138S0855	138S0750		ALL	4.7uF 0402	=> GRAPHICS (GPU)
311S00072	311S0657		ALL	Dual 2 INP AND GATE	
376S00122	376S0843		Q8450	NFET,30V.49A,PQFN8	=> PLATFORM POWER(PASS FET)
376S00124	376S00200		Q8470	NFET,30V.40A,8P DFN	=> PLATFORM POWER(PASS FET)
311S00118	311S0489		Q8601	DUAL INPUT AND GATE	=> POWER SEQUENCE
128S0444	128S0323		C4602,C4702	330UF, 6.3V D2E	=> USB-A
371S0718	371S0531		ALL	DIODE,BAT54,SHOTTKY,30V	=> POWER SEQUENCE
377S0124	377S0057		ALL	VARISTOR,6V8,2UA,100PF,	=> AC/DC POWER
138S0854	138S0762		ALL	CAP,1UF,20%,4V,X6S,0201	=> GRAPHICS (GPU)
138S00015	138S0777		ALL	CAP,10UF,20%,16V,X6S,0603	=> CPU&CHIPSET (CPU POWER) PLATFORM POWER (G3H_3V3.GPU)
138S0759	138S0762		ALL	CAP,10UF,20%,16V,X6S,0603	=> GRAPHICS (GPU)
138S0676	138S0691		C4100	CAP,22UF,20%,6.3V,X5R,0603	=> CAMERA
132S0325	132S0291		CA115,CA145	CAP,3300PF,10% 50V,X7R,0402	=> PLATFORM POWER (GPU)
131S00144	131S0825		C7018,C7031	CAP,CER,NP0/C0G,560PF,+/-2%	=> CPU&CHIPSET (CPU POWER)
152S1499	152S0864		L4102	IND,47NH,2%,1.3OHM,0402	=> SD CARD
107S00015	107S00011		R5400	RES,MTL FLM,0.00075OHM,1%	=> SENSORS(V/I)
107S0255	107S0240		ALL	RES,MTL FILM,.001OHM,1%	=> SENSORS(V/I)
107S0251	107S0249		R5520	RES,SENSE,0.002OHM,1W	=> SENSORS(V/I)
155S00115	155S00114		L3700	FERR BD,10 OHMZ,25%,8A	=> SSD
155S0659	155S0382		L5100	FLTR,EMI,FERR BD,30 OHMS	=> SMC
155S00007	155S0667		L3100/3200	FLTR,COMMON MODE,90 OHM	=> USB-C
155S0935	155S0667		L3100/3200	FLTR,COMMON MODE,90 OHM	=> USB-C
197S0588	197S0591		Y1101	XTAL,24.000MHZ,20PPM,9.5PF	=> CPU&CHIPSET (PCH)
197S0590	197S0591		Y1101	XTAL,24.000MHZ,20PPM,9.5PF	=> CPU&CHIPSET (PCH)
353S00711	353S2073		ALL	IC,INA210,CURRENT SENSE	=> SENSORS(V/I)
					=> SENSORS(V/I)
353S00712	353S2216		ALL	IC,INA211,CURRENT SENSE	=> SENSORS(V/I)
138S0684	138S0660		C3832	CAP,CER,10UF,20%,10V,X5R	=> HDD
353S00854	353S4342		U5100	IC,REF3330,V-REF,3.0V,5MA	=> SMC
353S4376	353S3384		U3800,U5700	IC,LMV331,COMP,OPEN COL,2.7V	=> HDD & PSU PCC
376S0977	376S00078		Q0600,Q5127	XSTR,FET,N-CH,DUAL,20V,	=> CPU & SMC
376S1129	376S00078		Q0600,Q5127	XSTR,FET,N-CH,DUAL,20V,	=> CPU & SMC
376S0972	376S00075		ALL	MOSFET,N-CH,30V,100MA	=> BT.SMC,USB,CAMERA,AUDIO
376S0855	376S00074		ALL	MOSFET,DUAL N-CH30V,100MA	=> HDD & SMC
132S00091	132S0429		C8453,C8492	CAP,CER,0.022UF,10%,50V,	=> PLATFORM POWER
371S00096	371S0595		DZ5550	DIODE,ZENER,3.0V,3.22V	=> SENSORS(V/I)
376S00167	376S0910		ALL	MOSFET NCH,30V,11.8MOHM	=> HDD & PLATFORM POWER
371S00095	371S0567		D6020	DIODE,SW,100V,.25A,2P	=> FAN
311S00116	311S0324		U2070,U2075	74LVC2G34GF/SS00	=> CPU&CHIPSET (PCH)
353S00992	353S2541		ALL	IC,OPA348,OP-AMP	=> SENSORS(V/I)
353S00993	353S2541		ALL	IC,OPA348,OP-AMP	=> SENSORS(V/I)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
311S0649	311S0541		ALL	2-INP AND GATE,SOT665	=> SMC
138S0748	138S0751		ALL	CAP,1UF,10%,6.3V,X7R,0402	=> GRAPHICS(GPU)
132S00057	132S0668		ALL	CAP,2200PF,10%,25V,X7R,0201	=> CPU&CHIPSET (CPU POWER)
132S00086	132S00045		C7006	CAP,X6S,0.022UF,6.3V,0201	=> CPU&CHIPSET (CPU POWER)
128S0368	128S0365		ALL	CAP,EL,AL,POLY,150UF,,BLK	=> PLATFORM POWER (3V3_S5/5V_S4)
138S00102	138S0773		CA130	CAP,1UF,10%,10V,X6S,0402	=> GRAPHICS (POWER)
138S0772	138S00013		C7561,CA661	CAP,2.2UF,20%,10V,X6S,0402	=> PLATFORM POWER
103S00185	103S0205		ALL	RES,1/16W,10KOHM,0.5%,0402	=> PLATFORM POWER (3V3_S5)
103S00186	103S0205		ALL	RES,1/16W,10KOHM,0.5%,0402	=> USB-C
103S00187	103S0205		ALL	RES,1/16W,10KOHM,0.5%,0402	=> USB-C
152S00403	152S00322		ALL	IND,0.68UH,20%,6.1A,	=> USB-C
138S0714	138S0713		ALL	CAP,10UF,6.3V,X5R,0402	=> USB-C
377S0178	377S00031		ALL	TVS,5.5V,7.3VBR,0.2PF,0201	=> USB-C
128S0311	128S0329		ALL	CAP,POLY,220UF,6.3V,35MOHM,B2	=> USB-C
138S00084	138S00060		ALL	CAP,47UF,20%,6.3V,X5R,0603	=> USB-C
152S00358	152S00208		ALL	IND,1.0UH,20%,2.0A,135 MOHM	=> USB-C
126-0312	126-0306		ALL	CAP,EL,100UF,35V,0.54A,THD	=> BLC
106S00017	106S4171		ALL	RES,MF,30.1OHM,0.125W,1,805	=> BLC
138S0758	138S0742		ALL	CAP,X5R,22UF,,MURATA	=> BLC
371S00043	371S00019		D6921	DIODE,SCHOTTKY,30V,100MA	=> PLATFORM POWER
155S00155	155S0441		L6000	FLTR,EMI,FER BD,220OHM,1.4A	=> FAN
371S0684	371S0495		D1900	DIODE,DUAL SCHOTTYKY,30V	=> CPU&CHIPSET (PCH)
155S0660	155S0513		ALL	FERR BD,22 OHM,25%,1A	=> AUDIO
					=> AUDIO
138S0641	138S0700		ALL	CAP,CER,X5R,2.2UF,10%,10V	=> AUDIO
138S0739	138S0706		ALL	CAP,CER,1UF,20%,10V,X5R	=> AUDIO
107S0184	107S0185		RT7000/1	THERMISTOR,NTC,200KOHM,1%,	=> CPU&CHIPSET (CPU POWER)
353S2970	353S2781		UA801	IC,SC4437,VOLT REF,3.3V	=> GRAPHICS(GPU)
107S00112	107S00006		RTA107	THERMISTR,NTC,47K OHM,1%	=> GRAPHICS(GPU)
311S00115	311S0302		UA102	IC,74LVC1G00,SNGL 2-NAND	=> GRAPHICS(GPU)
107S00041	107S00039		ALL	RES,MF,.0005 OHM,1%,150PPM	=> POWER & SENSORS
152S00388	152S00182		L6961	IND,PWR,2.2UH,20%,4.5A,43MOH	=> POWER
353S00831	353S00519		Q71X,72X,78X	IC,SIC621,DR MOS,IMVP-8,60A,	=> CPU&CHIPSET (CPU POWER)
107S0240	107S0255		R7800	RES,SENSE,0.001OHM,1W,4-TERM	=> CPU&CHIPSET (CPU POWER)
116S00007	116S00006		R2981	RES,MTL FILM,0 OHM,TIGHT TOL	=> USB-C
197S00046	197S00036		Y3000	XTAL,25MHZ,25PPM,20PF,50OHM	=> USB-C
197S00047	197S00036		Y3000	XTAL,25MHZ,25PPM,20PF,50OHM	=> USB-C
197S00048	197S00036		Y3000	XTAL,25MHZ,25PPM,20PF,50OHM	=> USB-C
353S00769	353S4398		U3510	IC,TPS22966,LOADSW,6A,5.5V	=> WIRELESS
155S0588	155S0367		ALL	FLTR,EMI BEAD,120OHM,3A	=> USB-A
138S0703	138S0648		C6302, C6305	CAP,CER,X5R,4.7UF,20%,6.3V	=> AUDIO
152S0098	155S0137		ALL	IND,CHP EMIFIL,1000OHM,0.2A	=> AUDIO & CAMERA
152S00543	152S00484		L8900	IND,MLD,0.24UH,20%,18A	=> GRAPHICS(GPU)
377S0184	377S00011		ALL	DIODE,TVS,BIDIR,5.3V,0.2PF	=> USB-A
138S1103	138S0719		C6309, C6310	CAP,CER,4.7UF,20%,10V,X5R	=> AUDIO
155S00076	155S0546		C6309, C6310	FER.BD,600OHM,25,300MA,	=> ETHERNET & CAMERA

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PAGE TITLE
ALTERNATE PARTS

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X646 BOARD SPECIFIC PHYSICAL AND SPACING CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,BGA_TBT,BGA_VRAM	MM	16.2

General Physical Rule Definitions

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.1 MM	0.070 MM	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
34_OHM_SE	*	Y	0.185 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
34_OHM_SE	ISL5,ISL8	Y	0.205 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
34_OHM_SE	TOP,BOTTOM	Y	0.220 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
39_OHM_SE	*	Y	0.150 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
39_OHM_SE	ISL5,ISL8	Y	0.165 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
39_OHM_SE	TOP,BOTTOM	Y	0.175 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
42_OHM_SE	*	Y	0.130 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
42_OHM_SE	ISL5,ISL8	Y	0.145 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
42_OHM_SE	TOP,BOTTOM	Y	0.155 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	*	Y	0.115 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	ISL5,ISL8	Y	0.126 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	TOP,BOTTOM	Y	0.135 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	0.090 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	ISL5,ISL8	Y	0.100 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.105 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	0.075 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	ISL5,ISL8	Y	0.080 MM	0.080 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
68_OHM_DIFF	*	Y	0.171 MM	0.085 MM	=STANDARD	0.130 MM	0.1 MM
68_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.085 MM	=STANDARD	0.150 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.136 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.141 MM	0.085 MM	=STANDARD	0.185 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.121 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.109 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.111 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.086 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.090 MM	0.085 MM	=STANDARD	0.230 MM	0.1 MM

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BGA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=STANDARD	?

Power and Common

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_ISO	*	=STANDARD	8000
GND_P2MM	*	=2:1_SPACING	1000
PWR_P2MM	*	=2:1_SPACING	1100

GENERIC

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GENERIC_ISO	*	=1:1_SPACING	?

BGA Area Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM

General Spacing Definitions

Default

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

Fixed and Dielectric

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1X_DIELECTRIC	TOP,BOTTOM	0.071 MM	?
1X_DIELECTRIC	ISL3,ISL10	0.101 MM	?
1X_DIELECTRIC	*	0.076 MM	?

Board Stack-up

FINISHED BOARD THICKNESS: 1.94 MM

_____	Top	Signal	0.5 oz (Cu plated)
_____		Prepreg	0.071 MM
_____	2	Plane	1 oz
_____		Core	0.101 MM
_____	3	Signal	0.5 oz
_____		Prepreg	0.115 MM
_____	4	Plane	1 oz
_____		Core	0.076 MM
_____	5	Signal	0.5 oz
_____		Prepreg	0.380 MM
_____	6	Plane	1 oz
_____		Core	0.076 MM
_____	7	Plane	1 oz
_____		Prepreg	0.380 MM
_____	8	Signal	0.5 oz
_____		Core	0.076 MM
_____	9	Plane	1 oz
_____		Prepreg	0.115 MM
_____	10	Signal	0.5 oz
_____		Core	0.101 MM
_____	11	Plane	1 oz
_____		Prepreg	0.071 MM
_____	Btm	Signal	0.5 oz (Cu plated)

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